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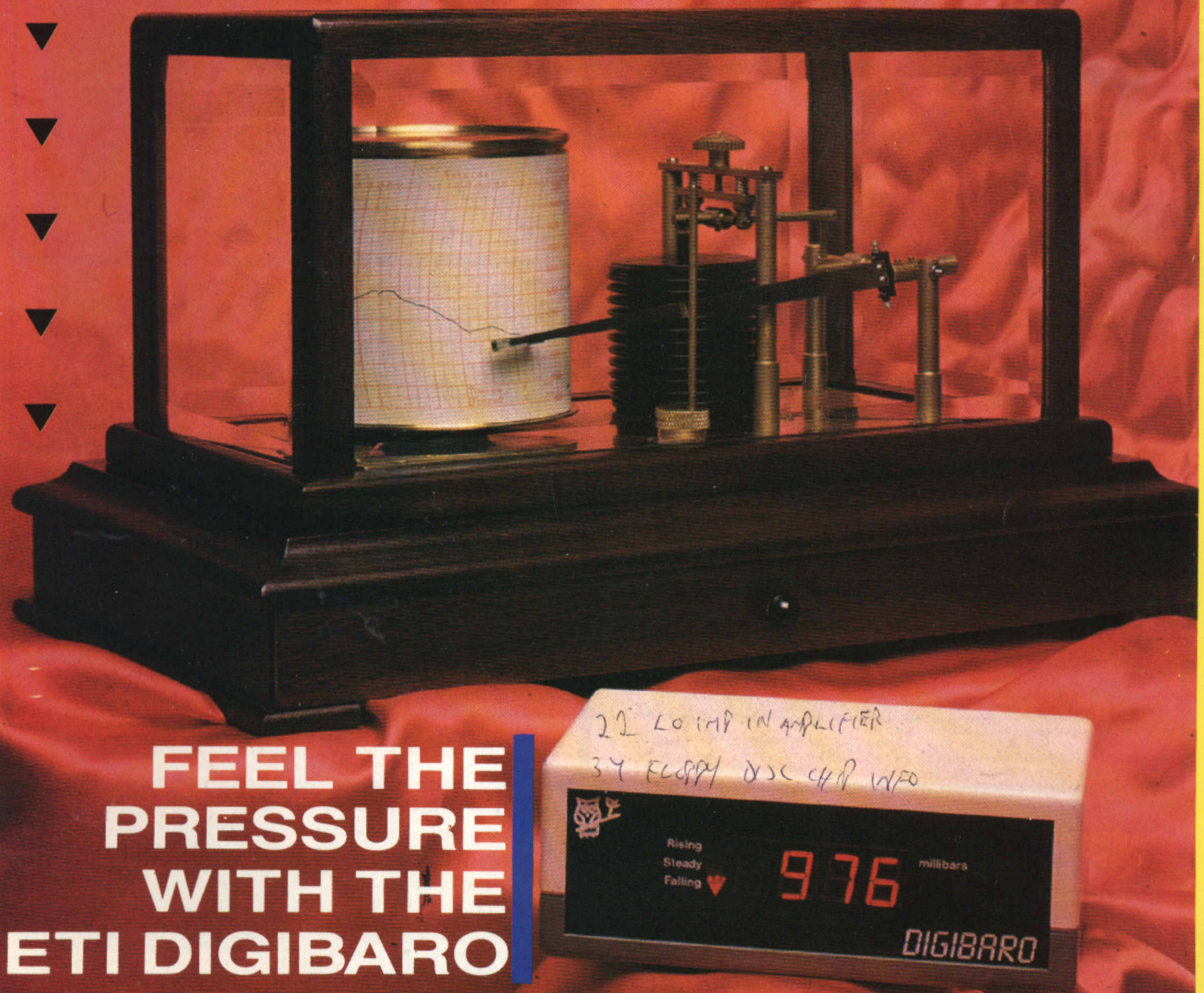

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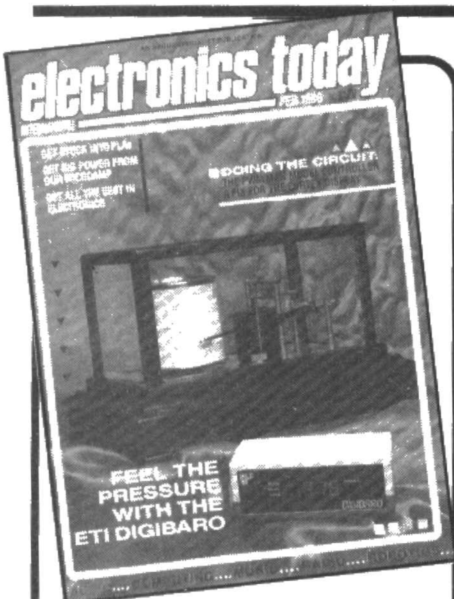

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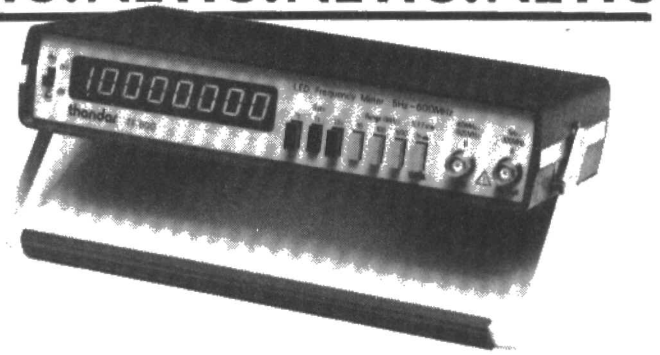
DIGEST



Thandar Competition Results

The competition in our November 1985 issue drew a large number of entries — not surprising, perhaps, when you consider that the prizes were three Thandar frequency counters and that the competition was very simple to enter. All that was required was a single word answer to each of seven doggerel rhymes, the construction of a certain word from the initial letters of the answers, and the completion of the phrase "I would like a Thandar frequency meter because . . ." in twelve words or less.

Almost everyone who entered correctly answered the seven doggerel rhymes, and even those who made the odd mistake or two were usually successful in the second section, identifying the seven letter word made up from the initial letters of the answers. The word, of course, was Thandar!

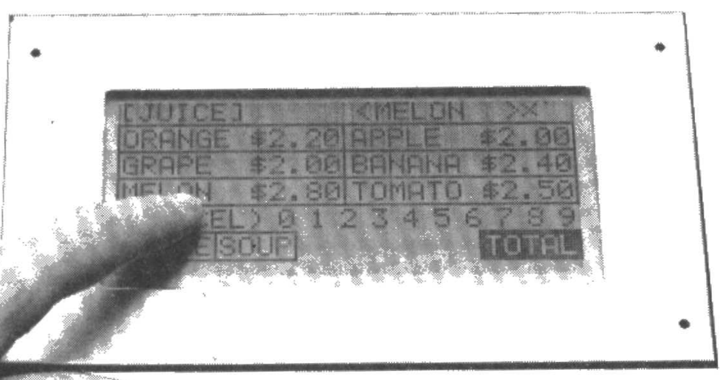
That left the tie-breaker, the completion of the twelve-word phrase. It quickly became clear that most of our readers have noted the appalling standard of our puns and are not above trying to outdo us. Just about every possible pun on the words count and counter appeared, with some people managing to cram two, three or even four puns into the twelve words.

Some of these were simply too tortuous to read, but among the better examples was that produced by Robert Marsh of Wisbey, Bradford, who said that he would like one of the prizes because 'I frequently meter time when I could count on one (That hertz!)'. Also worthy of an honourable mention is the solution submitted by Mike Salem of London NW1, who suggested that he could be '. . . using *Thandar and lightnening* my workload'!

There were plenty of others in much the same vein, but we eventually opted for the elegance and simplicity of the answer, 'I would like a Thandar frequency meter because I could count on it!'. This was sent in by C. Brook of 10, Stratford Road, Neston, South Wirral, who wins our first prize, a Thandar TF600 600 MHz frequency counter.

Among those who eschewed puns was John Crosby of St. Helier, Jersey. He chose to mirror the doggerel rhyme form in which the questions were phrased and came up with: 'Doggerel ditties you initially pitched, give me a counter, digitally switched.' We were also quite taken with the entry submitted by Andrew Bridgland of Hassocks, West Sussex, who said that he would like a Thandar meter because 'they have a nice, digitally-accurate readout'. The initial letters of this answer, you will note, form the word Thandar.

In the end, however, we selected two entries which we felt stood out from the mass of letters as being particularly different and memorable. P.T. Egan of 36 Epsom Road, Guildford, Surrey, wants a Thandar frequency meter because, as he tells us, 'It don't 'arf do your fingers in, using an abacus at 1GHz'. Similarly, few of the entries could match the simplicity and directness of that submitted by Karen Holloway of 49 Nether Street, Beeston, Nottinghamshire. 'I would like a Thandar frequency meter,' she said, 'becuase I like to know I'm right!'. These two readers will both be receiving Thandar PFM 200A 200MHz frequency counters.



Touch Key Overlays From Epson

Epson have developed a range of transparent, touch sensitive films which can be placed over LCD modules to provide a simple and direct means of entering information.

The Touch Key overlay comes in two different forms, an X/Y matrix version for applications requiring modest resolution and an analogue-to-digital conversion type for applications requiring higher resolution.

The X/Y type consists of two layers of transparent, conductive electrodes arranged as a series of stripes and laid one across the other on a glass film panel. Finger pressure at a given point causes the upper and lower electrodes to make contact and so enters the required information. This type is available now.

The ADC type also consists of a series of conductive, transparent stripes but has a uniform resistor block set at right angles to these stripes. The analogue-to-digital converter then converts the voltage measured across the panel into positional information. This version will become available during 1986.

Epson (UK) Ltd, Dorland House, 388 High Road, Wembley, Middlesex HA9 6UH, tel 01-902 8892.

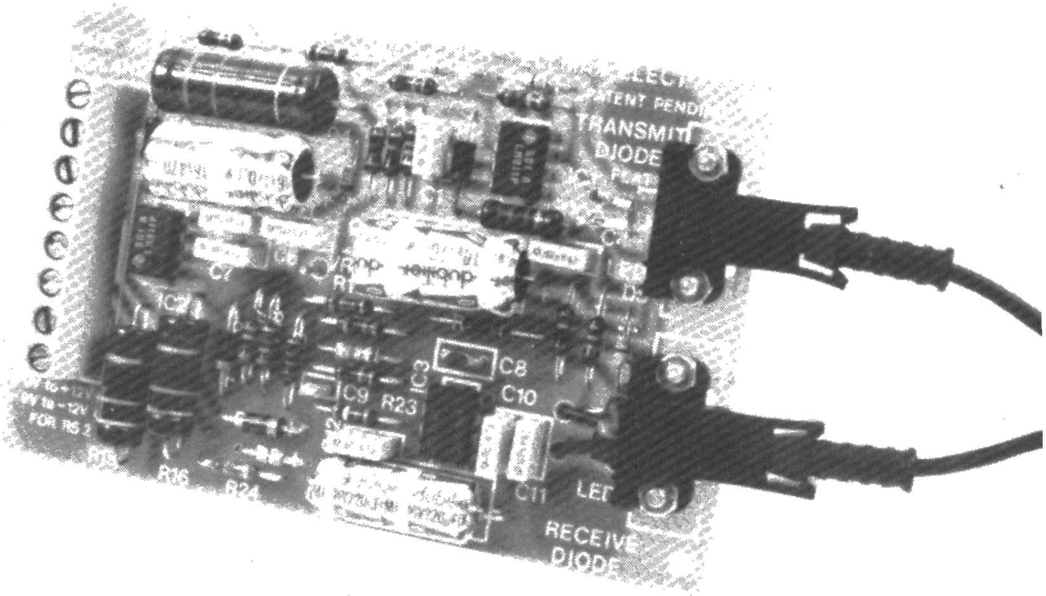
● **Coopers Cable Accessories have issued a 24-page catalogue which covers their range of cable marking and routing systems. It covers cable marking systems which allow figures, letters or symbols to be attached to cables from 7/0.2mm to 150mm² without the need to disturb wiring in situ, plus cable ties, cable clamps and bases, terminals, braided sleeving, spiral sleeving, conduit fittings and all the tools and accessories needed to use the products. Copies are available free-of-charge from CCA Ltd, Station Road, Studley, Warwickshire B80 7JS, tel 052 785 - 3514.**

● BICC-Vero have published a sixteen page full colour brochure which contains details of four different computer and terminal case systems. The cases are moulded from high impact polystyrene foam in oatmeal and bitter chocolate colour combinations. The brochure is called Workstation Packaging and is available free-of-charge. Also new is a 19" case system moulded from structured foam and available in 13 sizes from 3U to 12U. The case range is called Titan and details of it are available separately. BICC-Vero Electronics Ltd, Industrial Estate, Chandlers Ford, Hampshire SO5 3ZR, tel 04215 - 60211.

● *TI have published a reference book which describes the production and use of BIFET devices (semiconductors which feature both JFET and bipolar transistors on a common substrate). The BIFET Design Manual has sections on amplification, sampling, and filter and oscillator devices as well as data on individual devices and a section on miscellaneous circuits. It includes circuit diagrams, descriptions of the circuit operation and the design equations and in many cases explains the derivation of the equations. The cost is £5.45 inclusive from Texas Instruments Ltd, PO Box 50, Market Harborough, Leicestershire.*

● **Honeywell have produced a booklet entitled "Applying Manual Controls And Displays, A Practical Guide To Panel Design". It covers the basic ergonomic, aesthetic and functional considerations which must be taken into account when designing control panels and Honeywell say it brings together much useful advice on all aspects of man-machine interface design. For details contact Mike Kean, Honeywell Control Systems Ltd, Honeywell House, Charles Square, Bracknell, Berkshire RC12 1EB, tel 0344 - 424555.**

Low-Cost Fibre-Optics Transceiver



Ellmax Electronics have introduced a fibre-optics transceiver which operates at data rates from DC to 20K baud and can transmit over distances of more than forty metres.

The module contains both transmitter and receiver circuitry on a single PCB and uses a high-brightness, visible-red LED to transmit data along low-cost plastic fibres. Connections are provided for both CMOS and RS232 voltage levels.

The Fibre-optics transceiver costs £45.00 plus postage, packing and VAT.

Ellmax Electronics Ltd, Unit 29, Leyton Business Centre, Etloe Road, Leyton, London E10 7BT, tel 01-539 0136.

● **House of Instruments have published a 16-page, two-colour catalogue which describes their range of test and measurement equipment. It includes photographs and basic technical details of their oscilloscopes, counters, multimeters, function generators, and many other types of instrument, and copies are available free-of-charge from House of Instruments Ltd, Raynham Road, Bishop's Stortford, Hertfordshire CM23 5PF, tel 0279-55155.**

● *Ferranti have produced a comprehensive application report on their ZN433 analogue-to-digital converter. The report describes the construction of an evaluation board for the device and includes a full-size PCB pattern. The 433 is a 10-bit tracking ADC with a conversion time of 1us and Ferranti say it is particularly suited to applications where an input signal varies slowly but must be sampled often. Copies of the application report are available from Ferranti Electronics Ltd, Fields New Road, Chadderton, Oldham, Lancashire OL9 8NP, tel 061-624 0515.*

● Microlease have issued an update to their main equipment rental catalogue. It describes some fifty new items of test equipment which can be hired for periods of a week or more. For copies of both the main catalogue and the update, contact Sandie Petrie, Microlease PLC, Forbes House, Whitefriars Estate, Tudor Road, Harrow, Middlesex HA3 5SS, tel 01-427 8822.

New Company Makes Defence Research Available To Industry

Defence Technology Enterprises is a company which has been set up to help industry benefit from ideas developed as a result of research at selected Ministry of Defence Establishments.

Representatives of the company will be allowed to work alongside Ministry scientists at four establishments, Malvern, Farnborough, Portsland and Portsdown. By maintaining a close watch on research work they hope to be able to identify at source technologies which may have commercial potential.

Other companies who wish to gain access to the information collected by DTE will be able to become Associate Members. By paying an annual subscription fee based on their turnover, they will receive details of ideas related to their specific needs and requirements as well as regular bulletins on new developments, help in searching for answers to particular technical problems and assistance in obtaining finance to develop and enhance technologies revealed to them.

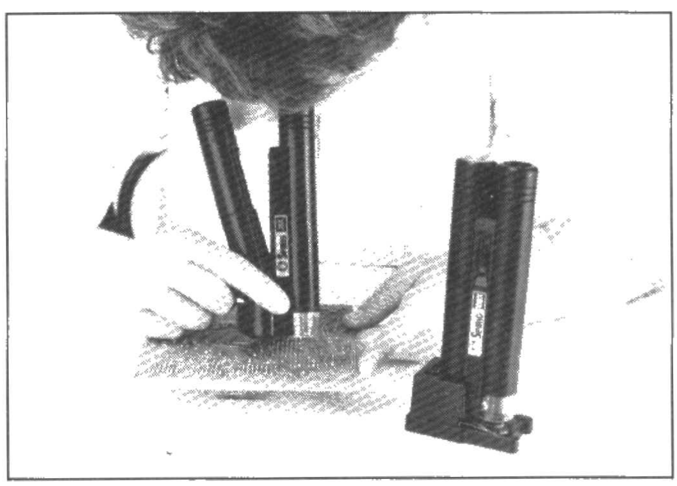
DTE will also provide assistance on a consultation fee basis for specific projects and, where technologies are likely to attract wide-ranging interest, will organise conferences and seminars. In certain circumstances, Associate Member companies may be allowed to send staff to work with scientists at Ministry research establishments or have MoD scientists seconded to them.

In a letter commending the launch of DTE, Secretary of State for Defence Michael Heseltine recalled several examples of defence research finding valuable civil applications. Among them were high resolution X-ray detector crystals which are used in body and brain scanners, liquid crystal displays, carbon fibre composite, and advanced aluminium lithium alloys. But, he argued, there is scope for greater and more systematic exploitation and DTE is the bridge between research estabishment and market place which will provide it.

The company is the result of an initiative by the merchant bank Lazard Brothers. Proposals for its formation were developed in conjunction with the MoD and seven other shareholders and given formal approval by the secretary of state. The company was launched on the 15th October 1985.

Illuminated Pocket Microscope

New from Cobonic is a self-illuminated inspection microscope which fits comfortably into the pocket and weighs just 4½ ounces. Powered by batteries, the microscope features adjustable focusing and is available with either 30x or 100x magnification. They cost £18.90 and £27.90 respectively and are available from Cobonic Ltd, 32 Ludlow Road, Guildford, Surrey GU2 5NW, tel 0483 - 505260.



Autowipe Kit

Cirkit have agreed to supply a complete kit of parts for the Autowipe project which appeared in ETI last month.

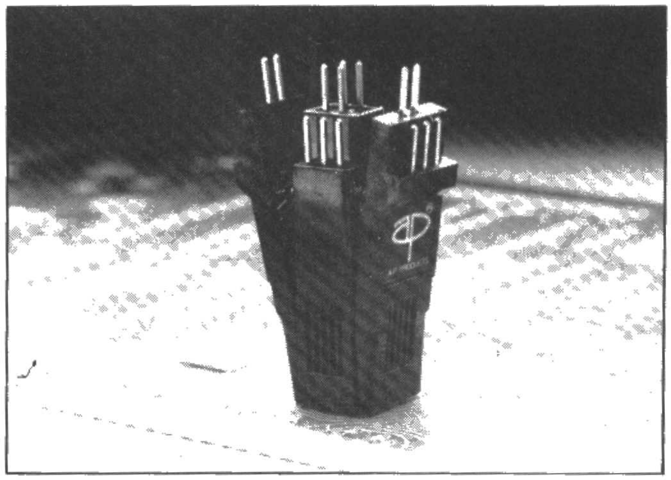
This variable speed windscreen wiper delay unit is unusual because it employs digital control and has a memory. The driver triggers two successive sweeps in the normal way and the Autowipe then remembers the interval between them and continues to operate the wipers at that interval until reset.

The kit will cost £11.80 plus 60p post and packing or you can purchase the PCB alone for £3.65 plus 60p post and packing. Please note that we will not now be supplying the board through our own PCB Service.

Cirkit Holdings PLC, Park Lane Broxbourne, Hertfordshire EN10 7NQ, tel 0992 - 444111.

● The Department of Trade and Industry have written to us regarding the Mastertronic Video+ which we described in the News Digest section of our October 1985 issue. The Video+ is a UHF amplifier and aerial system which is designed to broadcast the output from a VCR so that it can be picked up by nearby TV sets. In spite of Mastertronics' assurances that the legal position had been fully investigated, it now appears that retransmission in this way is illegal and that those caught using the system are liable to have the equipment confiscated and could face a fine of up to £2,000 or three months imprisonment. The DTI say they will shortly be introducing regulations to prohibit sale of the Video+.

● Vishay Mann have published a catalogue which covers their range of vitreous enamelled power rheostats. They offer resistances from OR5 to 10k with a standard tolerance of ±10%, power ratings from 12.5W to 300W and all products comply with MIL-R-22 standards. For further information contact Rod Myall, Vishay Mann Ltd, Wymondham, Norfolk, tel. 0953 - 602525.



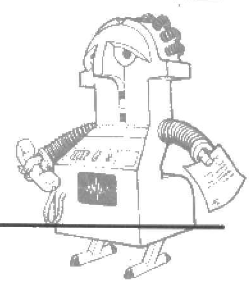
Surface Mount Test Clip

OK Industries have introduced a clip-on test connector which can be used with the plastic leaded chip carrier (PLCC) IC packages used on surface mount assemblies.

The 20-pin clip has the standard 0.1" contact spacing and uses a helical compression spring to ensure contact integrity The connections are brought out to a series of 0.025" square industry standard connector pins at the top of the clip. These are arranged in two rows at different heights to minimise the risk of shorting between test probes.

The clip costs £23.20 with alloy pin contacts or £30.93 with gold contacts. OK Industries UK Ltd, Dutton Lane, Eastleigh, Hampshire SO5 4SL, tel 0703 - 619841.

READ/WRITE



A Quick Conversion

Dear sir,

About twelve months ago I was showing a young friend how to make a simple speed controller for a model railway. He was soldering components in place while I looked on. During the conversation I mentioned that although the limit of my electronics knowledge was in front of him I had always wanted to make a synthesiser. His reaction resulted in the immediate cessation of the model railway scheme and the beginning of a long but eventually fruitful project. After several false starts, burnouts etc, the project began properly in March '85 and resulted in the completion of two inexpensive modular monophonic synthesisers.

Having explained that, I will move on to the reason for writing this letter. At the outset I was quite surprised to find that construction information was available at meagre cost, with no obligation to purchase kits or components. Helpful advice was freely given with occasions when staff and customers all pitched in together — it did not seem to matter whether I spent 20p or £20. Finally the return of post, first class, from suppliers was amazing.

I would like to thank all concerned at the following: Digisound, ETI, Emix, Lightning Electronics, Maplins and Technomatic.

In return for the above you have gained two more dedicated electronic music enthusiasts.

Yours faithfully,
Jim Read,
Birmingham.

Mr. Read was good enough to send us a photo of one of the synthesizers which, unfortunately, we can't print for lack of space. All we can say is 'thank you for your thanks'. — Ed.

ETI welcomes all queries, letters and contributions large or small. Any letter we receive is liable to be published unless marked 'Not For Publication'. We reserve the right to edit letters for reasons of space.

Please send any letters and contributions to ETI, ASP Ltd., 1 Golden Square, London W1R 3AB.

AUNTIE STATIC'S PROBLEM CORNER

Dear Auntie,

I have just finished building a DC-coupled audio amplifier but I can't take the project any further because I don't know how to adjust the 'DC offset' controls. What is DC offset and how do I adjust it?

Yours sincerely,
Edward Park,
London N7.

DC offset is a vague term with different meanings in different situations. In general it is used whenever the DC voltage in a circuit is not quite what you'd expect or when it has to be shifted for some reason. Rather than attempt a dictionary definition, I'll give you a few examples.

The DC level at the loudspeaker output of your amplifier should be 0V. If it is not at 0V, we can say that there is a DC offset at the output. This is not a desirable state of affairs because there will always be a current flowing through the loudspeaker, even when no signal is present at the amplifier input.

If the offset voltage — and hence the current — is small, the effect will be to bias the loudspeaker cone off centre so that its signal handling capability is reduced. Larger currents from greater offset voltages can cause overheating and permanent damage to the loudspeaker and crossover components. The DC offset controls allow you to adjust the DC output voltage to zero, to avoid these effects.

Another place you will often see offset voltages mentioned is in the specifications for op-amps and comparators. Here it refers to something slightly different: the input offset voltage.

An op-amp amplifies the voltage *difference* **between its inputs. If you were experimenting with op-amps for the first time you might very well expect that if both the inputs were at the same voltage, the output would be at 0V. It's what the theory says, after all!**

If you've actually tried it, you know that the output will swing to one or other of the supply rails because the circuitry of the two inputs can't be precisely matched in the op-amps characteristics. If you had a power supply that could be adjusted to give a few mV at the output, you could connect it between the two inputs and adjust it until the output of the op-amp was at exactly 0V. The voltage from the power supply would then be the input offset voltage of the op-amp — the voltage that must be applied between the inputs to obtain zero output voltage.

In many applications the input offset voltage of an op-amp will not be of much practical importance, but it does have a bearing on the way op-amp circuits are designed. Take a look at Fig. 1.

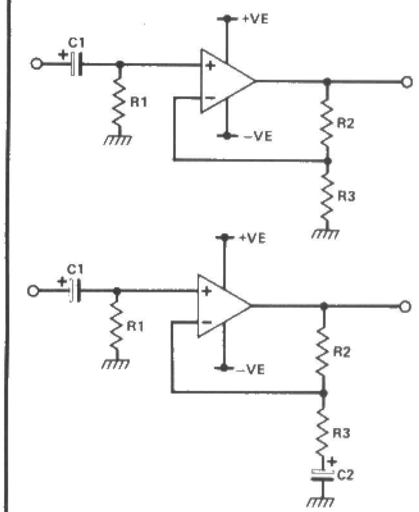


Fig. 1 Op-amp configurations

The two circuits are the same except that C2 is added in series with R3 in the second. Which is best? For a gain of 10 or so there's not much to choose between them; you could make a case for the second being marginally inferior because of the slight low frequency roll-off introduced by C2. If you are aiming for a gain of 1000, however, it's a different story. In the first op-amp circuit, the input offset voltage is seen as a DC input to the op-amp and will be amplified in the same way as a proper signal, so the output will be several volts away from 0V.

'Typical' offset voltages would be about 2mV for a bipolar op-amp (giving a 2V offset at the output), 5mV for a FET input op-amp, and 15mV for a CMOS op-amp (giving a 15V offset at the output!). Inclusion of the C2 prevents the input offset from being amplified, and so the second circuit is much better for high gain applications. — Auntie.

ETI

ALL ON BOARD

Barry Porter concludes his teach-in on PCB design.

Having arrived at an acceptable layout, you should now start again. Take another sheet of graph paper and draw the board outline and fixed components in ink. Then, being careful to follow your previous pencil layout, draw just the component outlines in ink. By separating the components from the confusion of tracks, it is possible to get a good idea of how the final board will look. At this stage you should be quite objective: are the components evenly spread out over the PCB area, or are they in overcrowded clumps, leaving large areas of unused board? Is everything as neat as it could be, or are there staggered rows of components and wire links all over the place? Are all the component dimensions accurate, so that everything can be correctly mounted? If you are not totally satisfied, now is the time to carry out any final corrections, so make any changes by drawing a new board outline, with the modified component placings, making sure that the movement of any component does not upset your carefully planned track layout. Once the final component positions have been established, the track layout should be added, using pencil or coloured ink, so that you arrive at a final layout master similar to the example shown in Fig. 8.

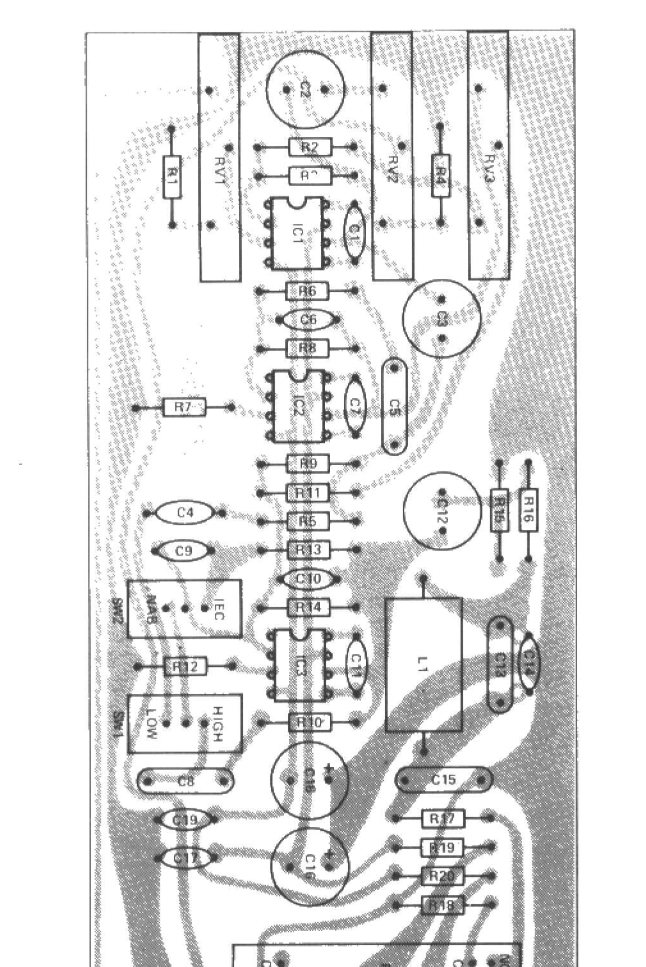


Fig. 8 The final layout from the component side

After a final check to ensure that the layout agrees with the circuit diagram, the first artwork master may be produced. Often referred to as the 'tape and dot' stage, this is simply a double-sided replica of the copper areas which will be on the finished circuit board, and is produced by sticking self adhesive opaque tape and other symbols onto a sheet of plastic drafting film, using the graph paper layout as a guide.

The first step is to lay claim to at least half the kitchen table (persuade junior that mud pies look much nicer on a bedroom window ledge) to which you firmly attach the graph-paper master with masking tape. Take a sheet of drafting film which is at least an inch larger all round than the circuit board outline and firmly tape this along its top edge so that it covers the graph paper layout. If possible, use drafting film which is matt on both sides. If yours has one shiny side, this should be kept as the underside.

Those who have only been reading this to find out why you were told to purloin some talcum powder, take heart — your moment has come. If your drafting film is typical of just about every other sheet of drafting film in the universe, it will be covered with enough greasy fingerprints to keep the whole of Scotland Yard amused for years. This being the case, take your precious powder (no, dear, you don't need the puff...) and give the sheet of film a light dusting and a quick rub with a piece of clean tissue before blowing any surplus in the general direction of the budgie's cage.

The Last Stage

You are now ready to begin the layout proper, for which you will require a supply of opaque adhesive pads, tapes and other shapes in an assortment of sizes. For working at a 2:1 scale, the following should be a minimum set:

- PADS: 0.2" diameter and 0.15" diameter (the smaller ones for ICs).
- TAPE: self-adhesive black crepe tape in widths of 0.06", 0.08" and 0.1".
- SHAPES: right angle elbows and T-pieces in the same three widths.

These materials should be available from any drawing office supplies shop.

The first stage is to place the pads in position on the film, and this is where a good pair of tweezers will prove invaluable. Make sure that each pad is placed accurately in place so that its central hole is aligned with the crossing point of the relevant graph paper lines. For maximum accuracy, the layout should be carried out over a precision grid placed on a lightbox. This *can* lead to mistakes, and the finished artwork should always be checked by placing it over the graph paper master. For most purposes, graph paper is sufficiently accurate to use as the guide for pad placement.

When all the pads are in position, place a second sheet of drafting film over the first, and place a further set of pads on this. Stick small pieces of 0.1" wide tape on each pad, covering the central hole. Draw in the corners of the circuit board, and you have created a solder resist mask. Return to the first 'dotted' sheet of film and add the interconnecting tracks, using suitable width tape. Where track density is fairly low, use at least 0.1" wide tape. For low impedance connections, such as earth or power supply rails, outline the copper area with tape and fill in with red transparent tape, which is considerably cheaper than track tape.

Having arrived at an acceptable layout, you should now start again ...

Don't forget to accurately mark the board edges — the accepted way of doing this is to mark each corner with a right angle using tape. Obviously, this is not necessary if copper is taken to the edge of the board. Be sure to show the scale of the artwork and finished board dimensions in an unambigious way. Always put a board name or number on the copper layout, as this ensures that you don't end up with back to front boards. If, as suggested, your layout has been carried out as viewed from the component side of the board, the annotation must be on the reverse side of the track artwork. Letraset or similar lettering should be used, and covered with a strip of matt adhesive tape for protection. Double-sided boards require a separate artwork for the top tracks, and this is easily prepared if the bottom artwork is used as a guide for positioning both pads and tape.

The component identification artwork requires a further sheet of film which should be placed over the graph paper master. Using a 1.0mm drawing pen, draw in the component outlines, using a stencil for small circles and a raised edge rule for straight lines. Unless your handwriting is up to ordnance survey standards, component identification numbers should be added by using a 3.0mm stencil and appropriate sized pen.

Once your artwork layers are complete, obtain a photocopy of the copper tracks on which to indicate the various hole sizes you require. As a guide to this, most resistor and capacitor mounting holes will be 1.0mm, and IC pads will require 0.6mm holes.

Now take your completed set of artworks and check everything at least twice before despatching them to your chosen PCB manufacturer.

Having just a few circuit boards made is not cheap, and a large proportion of the cost is in the photographic reduction work. This part of the process can often be carried out, at a considerable saving, by a friendly litho printing company who have their equipment in constant use and are usually less inclined to charge silly prices for what is, after all, a relatively simple operation.

Before placing your order with a firm of circuit board manufacturers, establish what their total charge is likely to be, and don't be afraid to admit to your lack of experience and/or money. They are the best people to advise you about board thickness and copper weight, and to point out any shortcomings with your artwork — but don't blame them if, after all your efforts, your first circuit board explodes with a cloud of smoke. When that happens, it really is 'back to the drawing board ...'. But it is still well worth the additional effort. It is a rewarding experience to turn out a good, well-planned circuit board. It's worth bearing in mind that there is no such thing as a professional circuit board designer who has not, at one time or another, made an error — so don't be too hard on yourself. If you really want to get it right, you may have to start from scratch and do it again until it is right. If you've been careful, and thought it all through, you'll get there, very probably on the first attempt.

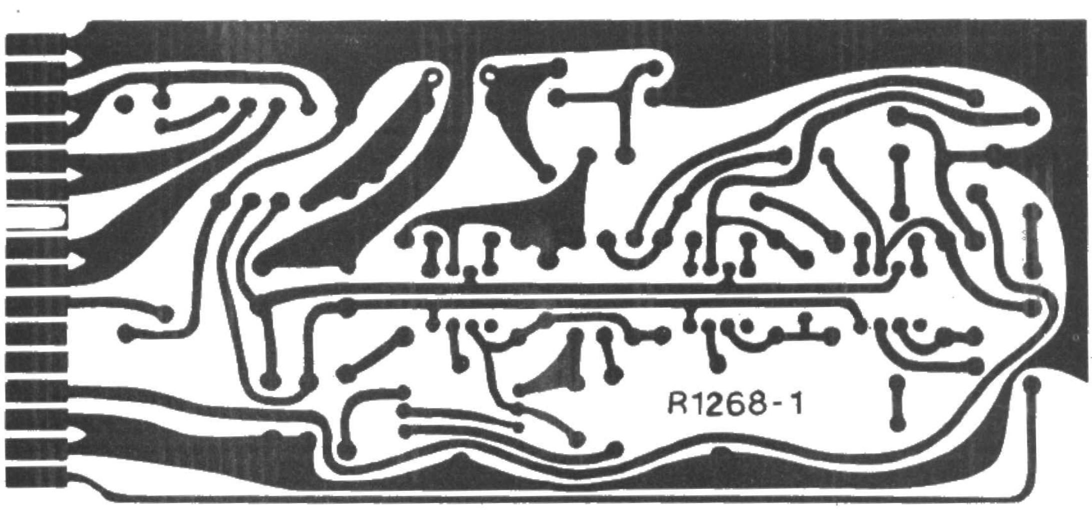


Fig. 9 The actual foil pattern — copper side.

ETI

DESIGNING TRANSISTOR STAGES

Les Sage concludes his investigation of simple transistor stages with a round-up of some useful two-transistor configurations.

So far all the circuits we've looked at have used only one transistor. A second transistor, however, can bring about a dramatic improvement in one aspect of circuit performance — if used judiciously.

Figure 9 shows a simple and economical method of achieving higher gain, just by running two stages together in series. Since neither stage has any emitter degeneration, the total gain (the product of each individual stage gain) can be very high indeed — around 5000 in this case. With such a high gain, it is important to keep the power supply smooth. In most applications, the power rail should be decoupled with a small series resistor and a parallel capacitor. It should also be noted that the DC operating point of each transistor is depdendent on its h_{FE} figure, so that R1 and R3 may need to be changed for individual transistors. General purpose NPN's are suitable, but each transistor will demand attention to these resistor values — so no recommendation has been made.

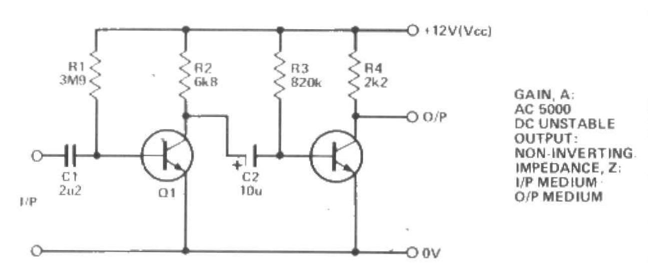


Fig. 9 Economic high gain amplifier. (Note: all circuits use general purpose silicon transistors operating at lower power AF or RF frequencies).

In fact, the circuit can also suffer from high distortion and demands low level signals in and out. Its only virtue is simplicity, and that is not outstanding.

A few extra components can make all the difference, as in Fig. 10. This is a universal gain block which finds many applications in audio equipment, particularly as an input stage in high quality amplifiers and as the basis of equalization stages. It utilizes the very high gain of a two-transistor stage to provide negative feedback (via R6). The eventual gain is considerably reduced, but the circuit is much less prone to noise, distortion and the idiosyncracies of transistors than that of Fig. 9.

The operating point of Q2 is set by the emitter resistor, R5, while R4 determines the open-loop output

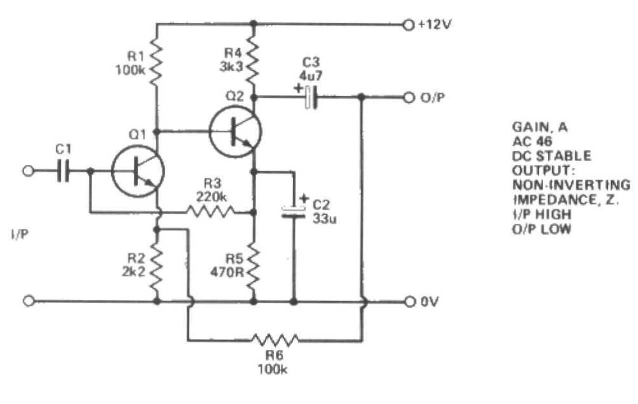


Fig. 10 Low noise, low distortion.

impedance (that is, assuming no feedback). DC feedback is run separately from AC feedback via R3. This biases Q1 and gives the circuit very good DC stability. R1 has a relatively high value to give the circuit low noise performance which is better than that of most op-amps. The feedback resistors, R6 and R2, set the overall gain at (R6+R2)/R2 (in theory, 46.45). The negative feedback through R6 also controls the input and output impedances. The lower R6 is, the more feedback there will be and the lower will be the output impedance. Lowering the value of R6 also increases the circuit's input impedance. This ability to determine a low output impedance and a high input impedance using one component is very desirable in audio circuits. It can also be exploited to design equalizing stages by replacing R6 with a suitable RC network, and such circuits are frequently found in RIAA equalizers.

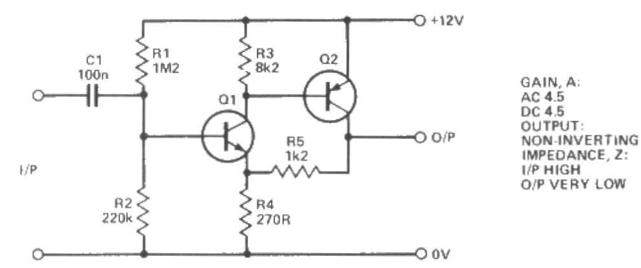


Fig. 11 Low gain, very low distortion.

Really Negative

Negative feedback is further exploited in the next two configurations. In the circuit shown in Fig. 11, the feedback is enormous, with the result that gain is very low and distortion is even lower. The circuit is popular in high quality pre-amps. With DC coupling as featured gain must be kept low in order to prevent DC operating point drift. The gain is actually determined by R5 and R4 and is given, approximately, by (R5+R4)/R4, If gain is altered by changing these values, then R1 and R2 will also need to be altered to bring the output DC point to around half the supply voltage. Like the previous circuit, this one features high input impedance (thanks largely to the negative feedback in the Q1 circuit) and low output impedance. In this case, the output impedance is very low at a few tens of ohms. Once again general purpose transistors can be used, remembering that Q2 is PNP and both transistors should be low noise varieties for audio work (BC182 and BC212, for example).

The next circuit (Fig. 12) features significantly higher gain at the cost of worse performance from the noise and distortion point-of-view. The circuit is very similar to that of Fig. 11, but has separate DC and AC feedback paths. The DC gain is unity and the AC gain (determined by feedback resistors, R4 and R5) is around 20. AC gain is given by (R4+R5)/R5 and can be adjusted over a wide range without significantly affecting the DC operating point.

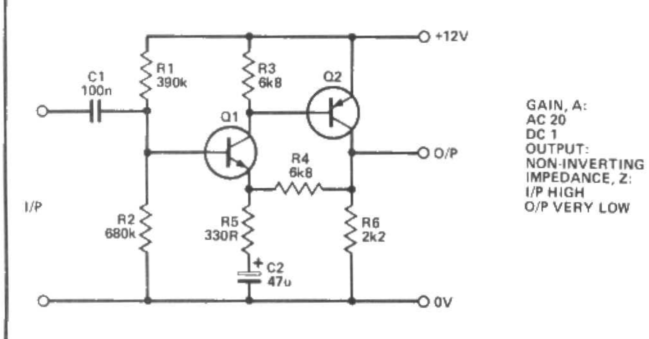


Fig. 12 DC stable, low distortion (Note: Q2 is PNP).

Distortion tends to increase with gain, but can be kept down by the use of complementary transistors (the BC182/BC212 pair would be suitable here). As with the Fig. 10 circuit above, frequency response can be tailored to the user's requirements by including reactive networks in the feedback loop. If the gain is lowered too much at HF, circuit stability might suffer with spurious oscillations as the result.

Both of the last two circuits depend heavily on feedback and may tend to oscillate if they are required to drive a large capacitative load. It is a wise precaution to include a small series resistor of around 100R at the output — especially if driving a screened cable.

Doing It With More Frequency

Amplifying frequencies above, say, 100kHz demands different techniques, as touched upon in discussing the common base amplifier in ETI, December 1985. Video frequencies go from DC to around 10MHz (although 5.5MHz is the maximum broadcast frequency) and we need to consider how to prevent deterioration of performance over such a considerable bandwidth.

The circuit shown in Fig. 13 has been designed with the main considerations for any high bandwidth amplifier in mind. Firstly, it features optimum collector current for maximum current gain/bandwidth product. An increase in emitter current (and therefore collector current) produces a decrease in the dynamic resistance of the base-emitter junction of a transistor *as viewed from the base.* This parameter is known as h_{ie} and is related to the dynamic resistance of the base-emitter junction as viewed from the emitter (or, r_e) by the following equation:

$$h_{ie} = (h_{fe}+1)\, r_e.$$

The decrease in h_{ie} with increasing emitter current follows from the approximate equation:

$$h_{ie} = (h_{fe}.25)/I_E$$

which itself follows from the relationship mentioned in the first part of this series (ETI, November 1985) between r_e and I_E:

$r_e = 25/I_E$, where I_E is in milliamps.

Unfortunately, as collector current increases the effective base-emitter capacitance also increases due to a phenomenon known as base-stretching. It is the base-emitter capacitance, C_{be}, which determines the high-frequency current-gain of a transistor and the cut-off frequency (the point at which transistor current gain falls by 3dB). The cut-off frequency, in fact, is defined as the frequency at which C_{be} and h_{ie} are equal, while the transition frequency, f_T (ETI, December 1985), is defined as the frequency at which current gain, h_{fe}, falls to unity. The transition frequency is roughly equal to the product of current gain and cut-off frequency.

Clearly, there will be an optimum collector current at which C_{be} going up meets h_{ie} coming down. In practice, this current is between 5mA and 50mA and is the value at which the transition frequency of the transistor is at its maximum.

Another consideration involved in the design of the Fig. 13 circuit is the inclusion of a low-level load resistor, R3. As well as helping to achieve optimum collector current in Q2, this serves to minimize the time constant of the output of the stage.

The circuit shown in Fig. 13 achieves a bandwidth of more than 40MHz although, like most video circuits, it is a heavy consumer of current. It also has a low input impedance. Transistor Q2 is configured as a common base amplifier giving a good voltage gain up to the transition frequency. It is fed by Q1 providing current gain alone and therefore not susceptible to bandwidth limitation. In fact, Q1 is configured as an emitter follower, giving a suitable low output impedance to match the subsequent stage. Resistor R3 provides a low load for Q2. The circuit resembles a standard cascode amplifier, but gives superior performance. It should be remembered that layout and supply decoupling are very important with any HF amplifier.

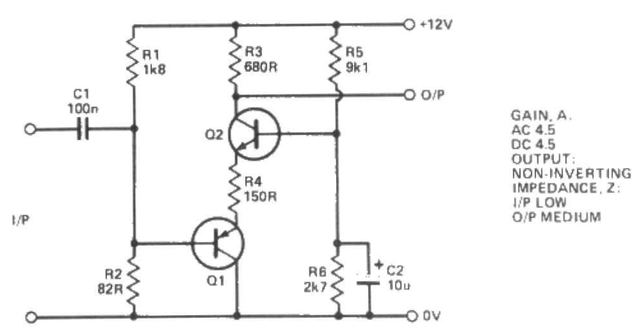


Fig. 13 Video amplifier (Note: both RF, Q1 is PNP).

The main drawback with this circuit is its use of series feedback to control the gain. Series feedback provides excellent bandwidth, but at the cost of increasing output impedance. Fig. 14 shows a circuit using two NPN transistors configured as common base and emitter follower stages and employing parallel feedback. Here, the feedback path is provided by R4 and R3. The circuit has a very low output impedance, although its high frequency response is weaker than that of the Fig. 13 circuit. The open loop gain of this circuit is given by R1/(R2//R_s), where R_s is the source resistance. Closed loop gain is effectively (R4+R3)/R3.

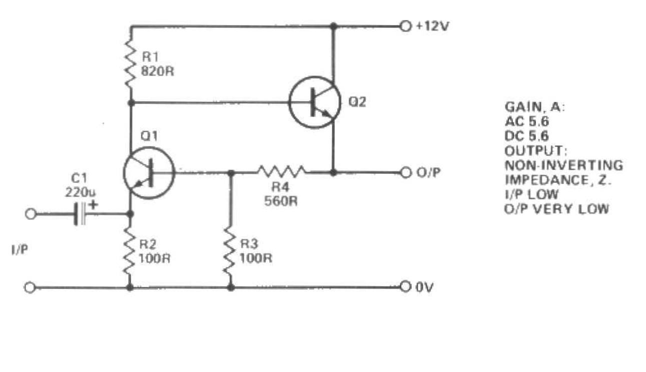


Fig. 14 Video amplifier.

The next circuit (Fig. 15) is a more-or-less conventional cascode amplifier with Q1 in common base mode and Q2 connected as a common emitter. The common emitter provides current gain and feeds the common base which provides voltage gain. The arrangement produces a high power gain. With the base of Q1 held at a constant voltage, V_{ce} for Q2 is also constant. This avoids the effects of Miller capacitance (ETI, December 1985) and so the normal deterioration of frequency response of a common emitter stage does not occur.

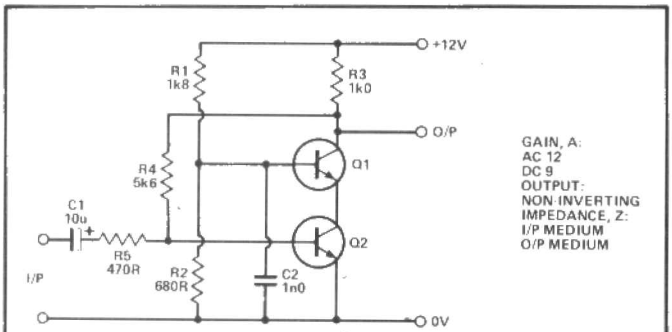


Fig. 15 Very linear cascode stage.

The configuration is widely accepted as a very high frequency amplifier displaying extremely good linearity. This feature is useful for quality audio, and the circuit can often be found in amplifier systems.

In this circuit, gain is controlled by parallel feedback via resistor R4, lowering the open-loop output impedance and successfully stabilizing the circuit. Improved frequency response can be obtained by omitting R4, short-circuiting R5 and placing a resistor in the emitter of Q2 to provide series feedback. This will increase both the input and output impedance.

Vive La Difference

The circuit shown in Fig. 16 is commonly called a differential (or operational) amplifier, although it was once universally referred to as a 'long-tailed pair' in deference to the joint emitter resistor. In this configuration, the input signal is applied across the two input terminals and the output is taken from across the two output terminals. If there is no potential difference across the two inputs (both being positive for conduction to take place) and assuming the transistors and collector resistors are identical, then both halves of the circuit will conduct equally and there will be no difference across the output terminals. The input here is described as common mode. Referred to ground, each output terminal produces an inverted version of the input at a gain given by the ratio of one collector resistor to twice the tail resistor (in the example, about unity).

Now, imagine that input 1 is made slightly more positive than input 2 — either by increasing the applied DC voltage or through the application of an instantaneous AC voltage. More current will flow in the collector-emitter circuit of Q1 and the voltage across R1 will increase. Referred to ground, the voltage on output 1 will fall and a potential difference will appear between outputs 1 and 2. This potential will be proportional to the potential across the inputs and will be inverted (output 1 voltage decreasing as input 1 voltage increases). The same reasoning applies if input 2 voltage is changed, with the net result that the output of the circuit will be proportional to the potential difference across the input terminals.

Assuming that the tail resistor is large enough (much greater than the dynamic emitter resistance of the transistors, r_e), then the potential drop across the inputs can be expressed in terms of emitter current and $2r_e$. In this way, it becomes clear that the output can be taken from only one collector with reference to ground and still be proportional to the potential difference across the two inputs.

In fact, this depends on the tail resistor acting as a constant current source, which it will do if it is large enough. Looked at in this way, the voltage drop across the resistor remains constant and the current flowing through it remains constant — which actually applies only when small voltage changes take place. As long as R3 can be considered a constant current source, any change in collector and emitter current in one transistor will be exactly matched by an opposite change in the other. Current is diverted to whichever transistor is more heavily biased into conduction and, using a single-ended output, one input becomes an inverting input and the other non-inverting. In effect, R3 is decoupled to difference signals across the input terminals while common mode signals produce a voltage across it thereby providing negative, gain-reducing, feedback.

For difference signals, the differential amplifier has a very high gain, given approximately by the formula $10I_TR_1$, where I_T is tail current and R_1 is one of the collector resistance values. The compromise involved here is due to the fact that, in our circuit, a high tail current is incompatible with a high tail resistance value. In practice, differential amplifiers tend to be designed with genuine current sources in the tail (usually a fully stabilised transistor circuit producing a quiescent collector current).

The most important feature of differential amplifiers is their common mode rejection, which ensures that thermal noise, drift and any similar voltage disturbances common to both transistors are ignored during amplification. The measure of a differential amplifier's quality is its common mode rejection ratio (CMRR), given by the ratio of difference signal gain to commmon mode gain and usually expressed in dBs. In the Fig. 16 circuit, the

CMRR would be between about 20 and 40 dBs — an unimpressive figure, given contemporary op-amp CMRRs in excess of 100dBs. The simplest way to improve the CMRR would be to increase the value of R3, but this would require higher supply voltages (or even a split rail supply) to maintain tail current.

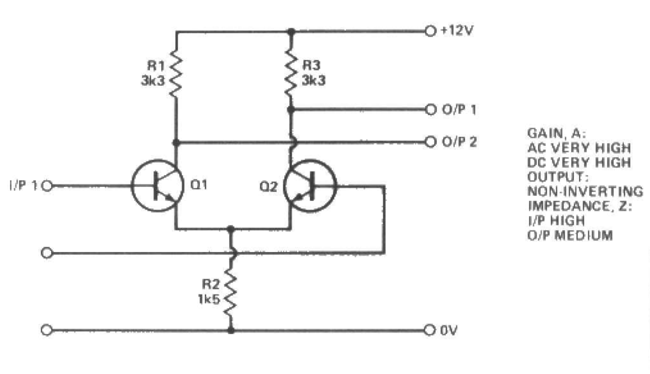


Fig. 16 Basic differential amplifier.

Conclusion

The few circuit blocks described in this series should show the wealth of design opportunities for those willing to work with discrete components. The important thing to remember is that a circuit can be readily designed for practically any given purpose, if first you are clear as to the requirements that will be made of it. Once the general outlines have been understood and a configuration decided on, the calculation of component values can proceed with recourse to little more than Ohm's Law. Rather than tie yourself up with complex mathematics (unless, of course, that is what you enjoy) a circuit block can be produced with the aid of some common sense, a few rules of thumb, a few sums and a clear idea of what you want. The final stage in the process, of course, is to build your design and test it. You will, undoubtedly, find that minor adjustments need to be made to your component values, but if you pay heed to the advice that a little observation and measurement is worth a ton of theory you will almost certainly produce circuits which work and work well. The theory may produce working circuits, but only the practice will make them perfect.

ETI

AUTOMATIC TEST EQUIPMENT

Analogue electronics is considered by many electronic engineers to be a black art, and the testing of analogue circuits even darker. W.P. Bond casts a little light.

Because of the specialized nature of most analogue circuits, the main limitation on their design is the ingenuity of the designer. It is difficult to lay down any single technique which would work for all possible analogue circuits. The automatic test equipment used to test analogue circuits must allow for a variety of different techniques and has to be capable of being modified to provide a range of input stimuli and response measurement configurations. Such ATE is usually described as modular.

Modular ATE will incorporate a standard instrument bus (most commonly, the IEEE 48 or General Purpose Interface Bus, GPIB) and all the test instruments required can be hung on the bus. The instruments are controlled by the ATE program and are routed to the unit under test (UUT) by a set of scanners — for example, a relay matrix. Each instrument can be considered a module of any given testing configuration. Each testing configuration would employ a particular set of modules —typically including programmable power supplies, programmable DC sources, an AC source, a digital voltmeter, general purpose or reed relays, a phase angle voltmeter and logic units to perform drive and sense functions. Specialist modules would include spectrum analysers, synchro sources and pulse generators. For obvious reasons, such a modular system is often referred to as 'rack and stack', and a typical configuration is shown in Fig. 24.

Having A Breakdown

The circuit to be tested is broken-down into functional blocks for which we have defined test procedures. Figure 25 shows a basic block layout for a data acquisition subsystem, consisting of input buffering, input multiplexing, sample and hold, analogue-to-digital conversion, output buffering and control/decode logic.

This last block should be tested first in any circuit in which it features. Signature analysis (ETI, December 1985) or static truth-table testing could be used. Input buffering and multiplexing come next and are tested for insertion loss and crosstalk errors. All MUX inputs are grounded and the addresses are stepped through in sequence until all channels have been selected.

Insertion loss results from the inclusion of networks and functional blocks in a signal path. It can readily be measured by comparing output with input (voltage, current or power) and if the result is outside acceptable limits, the measurement can be interpreted as indicating a fault within the network or functional block. Similar comments apply where insertion *gain* might be expected from the inclusion of amplifying stages in a circuit.

In our example, the output of the multiplexer would be monitored assuming a fixed input. If the analogue-to-digital converter in the circuit operates at a full-scale (FS) of 10V, insertion loss might be tested at +FS, –FS and 0V. The limit for acceptable loss in this sort of circuit would usually be set at the voltage equivalent of one least-significant bit (1 LSB) — with a 12-bit bipolar ADC operating over a 20V range this would be 20V/4096 or 4.88mV.

As each channel is tested for insertion loss, the other inputs are grounded. Tests for input shorts and multiplexer selectivity (channel isolation or crosstalk) can be carried out at the same time since, if any channel is not isolated when another is selected, the output of the multiplexer will be loaded. Pin faults can also be detected during this procedure.

The sample and hold (S-H) circuitry is tested next. Its function is to hold the instantaneous (sampled) input voltage constant while the ADC is converting it. All tests after the MUX will usually be made with a signal routed through one particular channel so that known channel losses can be accounted for and kept constant. In testing the S-H block, it is desirable to have low offset in sample mode with 0V and +/–FS as suitable input voltages. Acceptable errors are specified in manufacturers' data sheets. It is easier to check S-H hold performance by perfoming a conversion than by dynamically measuring the drift.

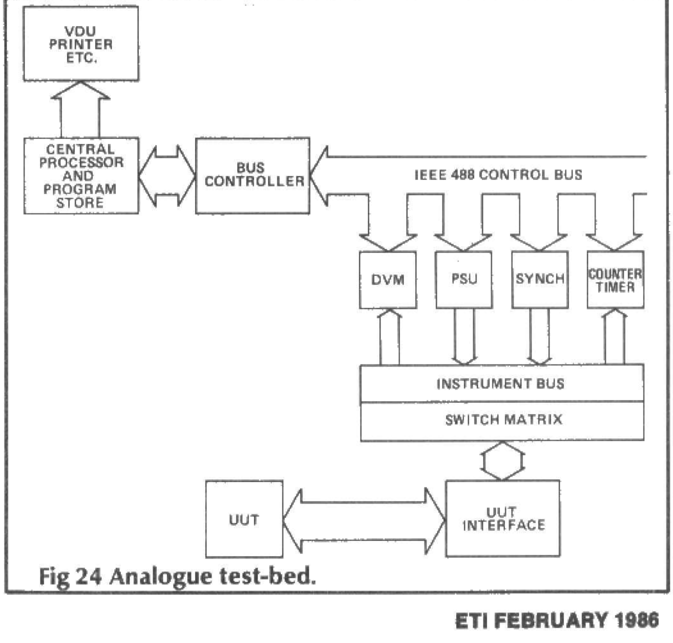


Fig 24 Analogue test-bed.

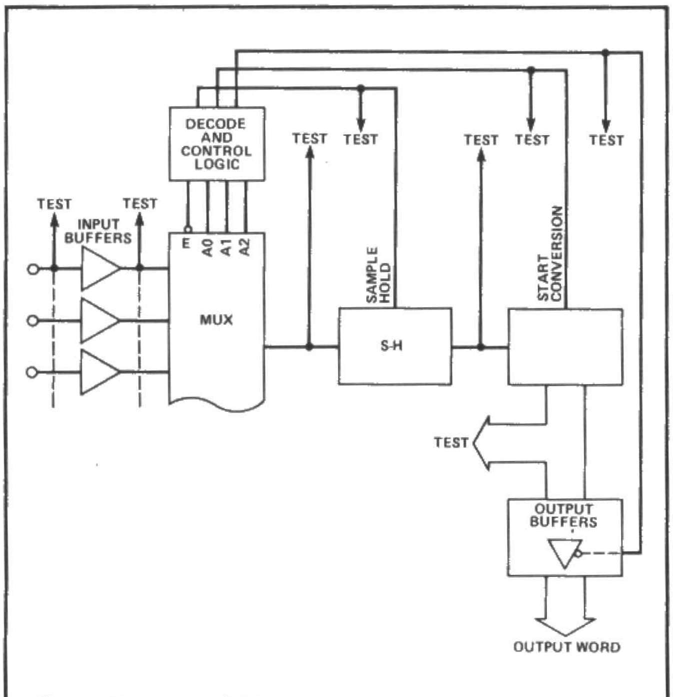


Fig. 25 Data-acquisition system.

Testing The Converter

A comprehensive test on an ADC block can be very complex. First, offset and gain adjustment should be set according to manufacturers' directions. After adjustment, the 0V offset should be tested to check that it is within 1 LSB. Offset (or zero scale) error is a measure of the difference between theoretical and actual behaviour of an ADC at zero input voltage. As Fig. 26b shows, the effect is to shift the transfer characteristic of the ADC to the right or left. Offset is determined as the difference between the theoretical and actual input voltage at which the output of the ADC switches from zero to one bit and can be expressed as a percentage of the full-scale voltage. It is usually adjusted to ½ LSB, at which value quantization error is minimized.

Gain (or full scale) error is a measure of the difference between the theoretical and actual behaviour of an ADC at an input equal to full-scale (Fig. 26c). The effect is to rotate the ideal transfer characteristic about the origin. The error is determined as the difference between the theoretical and actual input voltage at which the output switches to full-scale and is expressed as a percentage of FS. Gain error is sometimes adjustable to zero in the circuit, but where it is greater than 1 LSB and is not adjustable, it will have to feature in later calculations.

The single most important error when it comes to determining the performance of an ADC is linearity error. It is a measure of the maximum deviation of actual performance from the theoretical straight-line (Fig. 26c). It is an intrinsic feature of the ADC and cannot be adjusted, and it should be measured after offset and gain have been calibrated. It is expressed as a fraction of LSB or as percentage of FS and it is tested for by checking actual ADC output against expected output for a range of definite input voltages. The number and value of the test voltages are fixed only by the degree of accuracy desired.

The final test for ADCs is for differential non-linearity (DNL) which will reveal missing codes. Differential non-linearity implies that the ADC will display non-monotonic behaviour and it is, if it exists, an intrinsic feature of the particular ADC. The ideal step size for any ADC is 1 LSB. A deviation from this ideal may result in some codes not appearing at the output at all (Fig. 26d). The important parameter is code-width — that is, the voltage range over which a given code will be output. It should be clear that a code width of 1 LSB gives a differential linearity error of zero — in other words, it will result in exact bit-wide steps. A code-width of between ½ LSB and 1½ LSB gives an error of ½ LSB, which is usually acceptable. If the code-width is less than ½ LSB or greater than 1½ LSB, then — to all intents and purposes — the same code will be output for more than one transition voltage. In other words, there will be missing codes.

Testing for code-width usually demands a programmable DC voltage source with a high resolution (at least 1mV). By gradually incrementing the voltage applied to an input in, say, 1 mV steps it is possible to count the number of steps between actual transition points and compare the count with the theoretical code-width representing 1 LSB in mVs. An error can then be used to generate a fault message. The accuracy is dependent on the precision with which the transition voltages can be determined. Differential non-linearity only relates to adjacent codes. In order to obtain a comprehensive idea of the DNL of an ADC it is, of course, necessary to test at every transition point.

The final test in our example circuit would be on the output buffer. The required procedures have all been dealt with before, so I won't repeat them. The principles outlined above for testing analogue units can be readily modified for the testing of practically any such module.

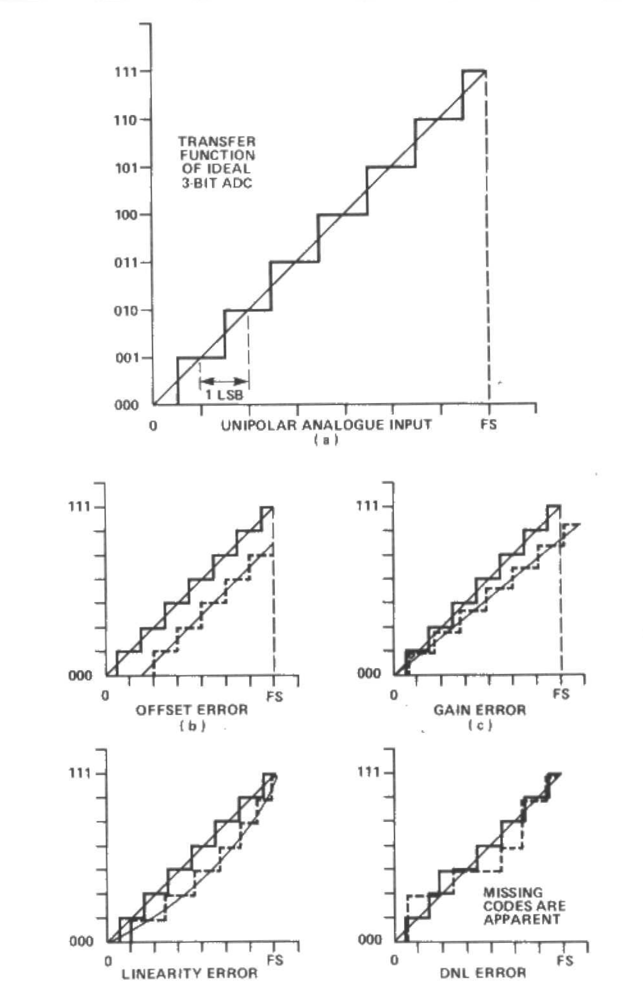
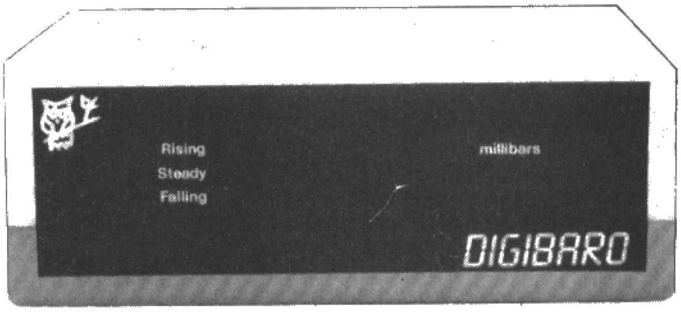


Fig. 26 ADC errors.

ETI

THE DIGIBARO

Raise your glasses to a digital barometer design from Ken Wood.



The Digibaro is an electronic barometer which provides a digital readout of atmospheric pressure over the range 845 to 1098 millibars. It is temperature compensated, operates from the mains, and includes a separate LED display to indicate whether the pressure last rose, fell or has remained steady. Adjustment is provided to allow it to be compensated for height above sea level.

Figure 1 shows the block diagram of the Digibaro. The output from a silicon piezo-resistive pressure sensor is amplified and fed to some conditioning circuitry which provides the temperature compensation. The output is then fed to an analogue-to-digital converter. The display system consists of a four digit multiplexed LED display, decoding being performed by the program in an EPROM. The trend of any pressure changes is detected and also decoded by the EPROM.

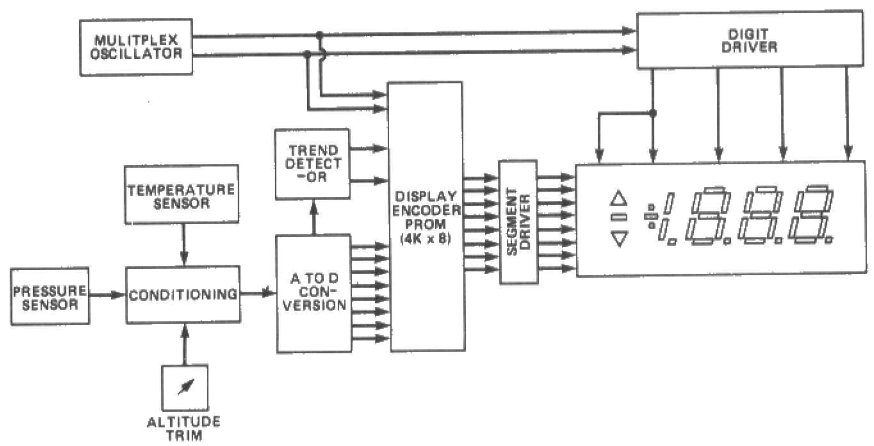


Fig. 1 Block diagram of the Digibaro.

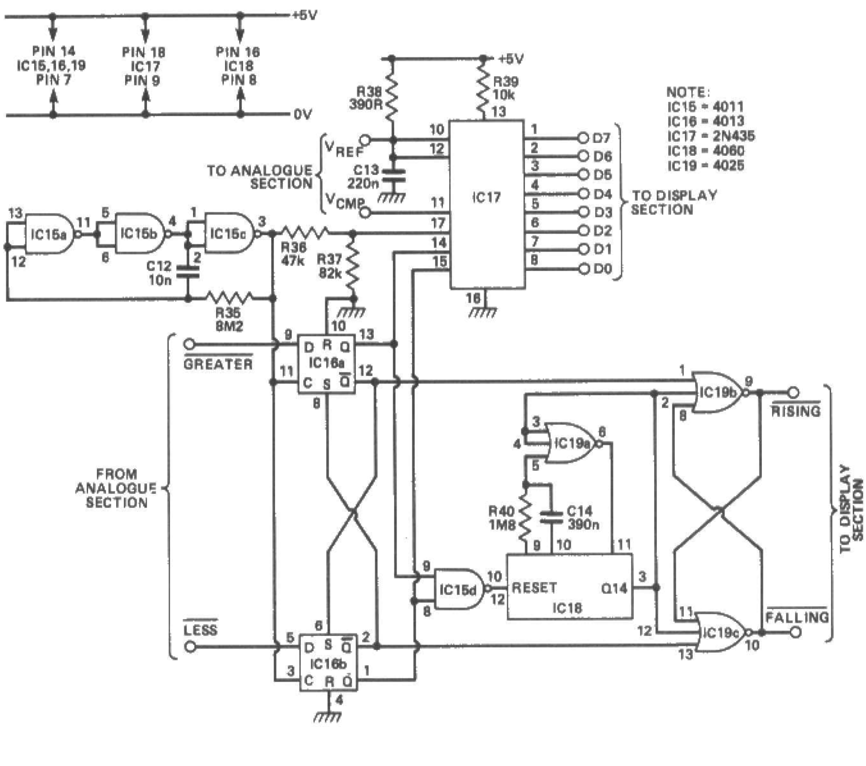


Fig. 2 Circuit diagram of the digital section.

Construction

The circuit boards have been designed to fit a snap-together plastic Verobox, which gives the finished project a neat appearance. Other enclosures could be used if required.

The first step is to check the mounting arrangements for the transformer. The transformer may be mounted in three ways — on the PSU board, on the back panel of the box, or in the base of the box. Mounting it on the aluminium back panel will improve heat transfer, but in the prototype the transformer was mounted on the PSU board. Connections are available for a PCB mounting transformer, but if one of these is used it is recommended that the

HOW IT WORKS

The power supply is in three sections, one for each of the other parts. The digital and display sections are both fed from the same winding on the transformer via BR1 but have independent regulator circuits. The analogue section requires positive and negative supplies, and these are provided by IC1 and 2 and capacitors C1–4. The supply for these is obtained by a slightly unusual voltage summing network, D1 and 2 and the other secondary of T1.

The pressure sensor (IC11) must be compensated for temperature drift and its output amplified from about 60 microvolts per millibar to the 10mV/mb required to operate the A/D converter. IC9 produces a voltage which depends on temperature, and IC10a uses the stable voltage reference from the A/D converter to produce a voltage which varies in the opposite direction. By mixing the two together a voltage with any percentage drift with temperature may be produced, and used to cancel the effects of IC11 and the rest of the circuit.

The supply to IC11 is controlled by IC10b and trimmed by RV1 to cancel the major sensitivity of the IC. The differential output is amplified by IC12a and again by IC12b which also subtracts an offset (adjusted by RV2 and RV3) from the sense voltage. This compensates for fixed offsets in IC11, pressure variation with altitude, and the fact that the voltage to the A/D converter is zero for 844mb.

The overall amplification is trimmed by RV4 and noise removed by R30/C11. IC13 and 14 compare the voltage produced with the output of the A/D converter and control whether it counts up or down.

The A/D converter is actually a D/A converter used in a feedback loop with a couple of comparators and a counter. The counter and D/A converter are contained in IC17, and the counter is clocked by the oscillator built around IC15a, b and c. The counter tracks the input voltage by counting up, down, or not at all according to the command from the comparators. The command is synchronised to the clock by IC16 so that it can be used by the trend detector.

Any change causes the counter IC18 to reset, and registers its direction at the RS latch formed by IC19b and c. If, after a time, there has been no change, the output of IC18 will go high, disabling the RS latch and the counter's internal oscillator. Any further change will start everything up again.

The display section has been designed to be as flexible as possible. The four digits are multiplexed and scanned by oscillator IC5 and decoder IC7. The scan outputs also control the decoder EPROM IC6, which generates the correct data for each digit. The outputs of the EPROM are buffered by IC8. The EPROM is programmed to show the trend and mb display or to give out-of-range indications. The multiplex scan is available off-panel for other applications or may be generated elsewhere by omitting IC5.

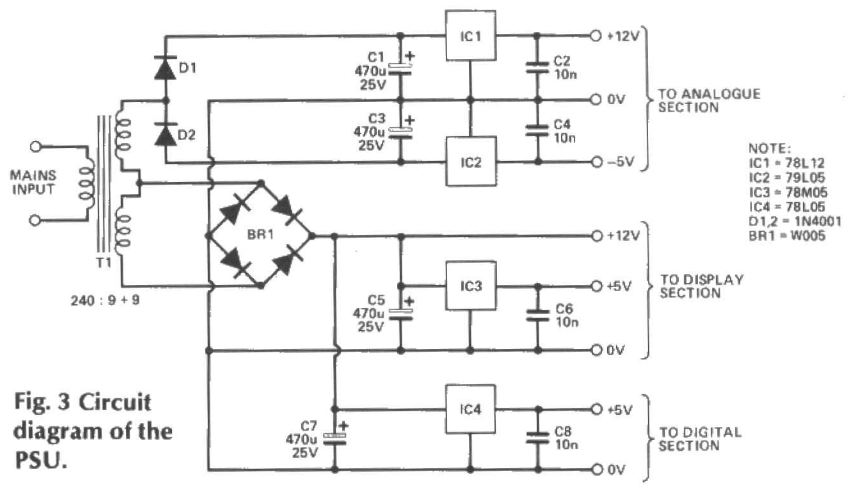


Fig. 3 Circuit diagram of the PSU.

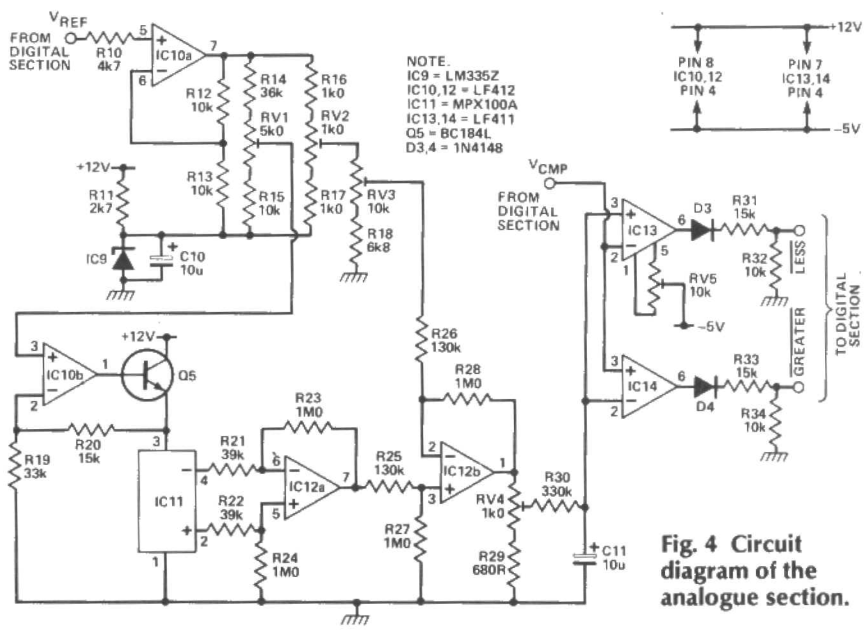


Fig. 4 Circuit diagram of the analogue section.

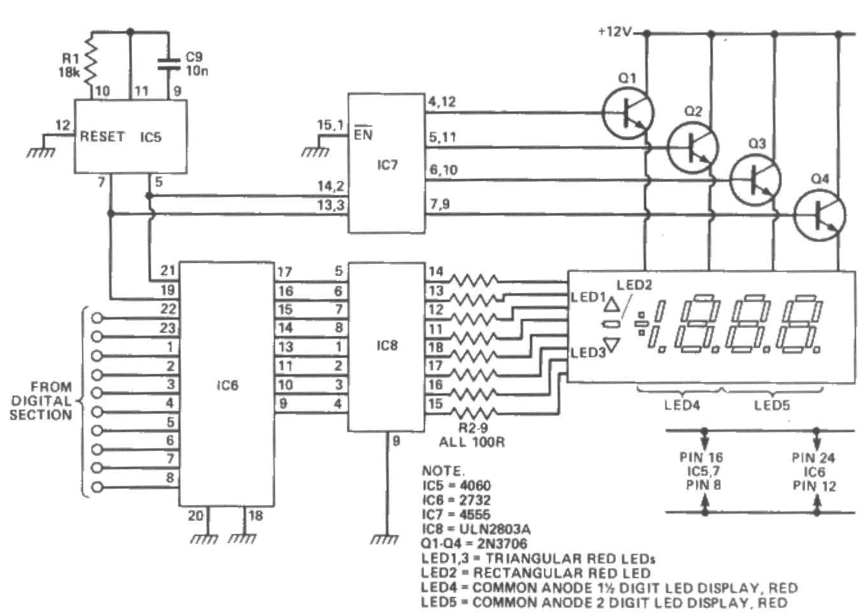


Fig. 5 Circuit diagram of the display section.

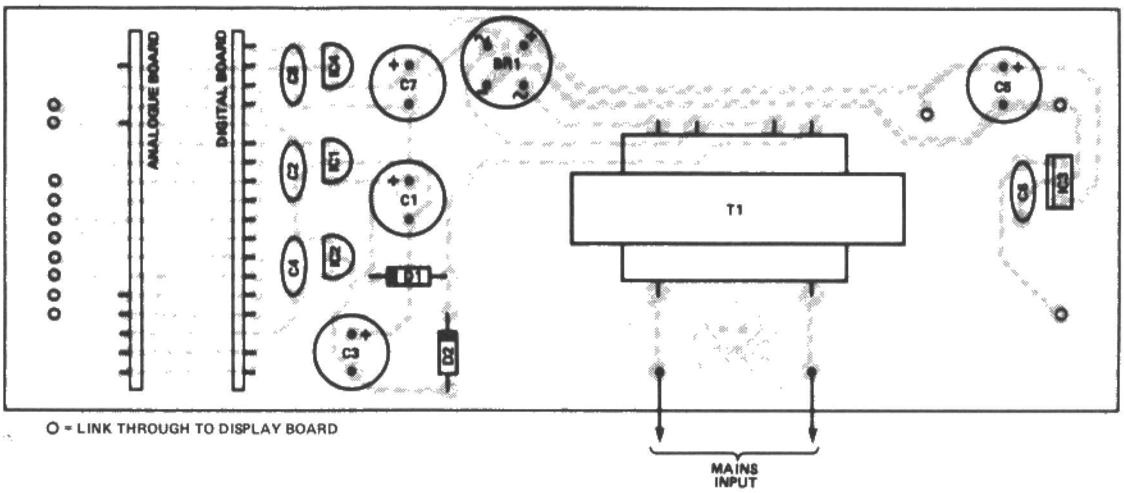


Fig. 6 Overlay diagram for the PSU/motherboard.

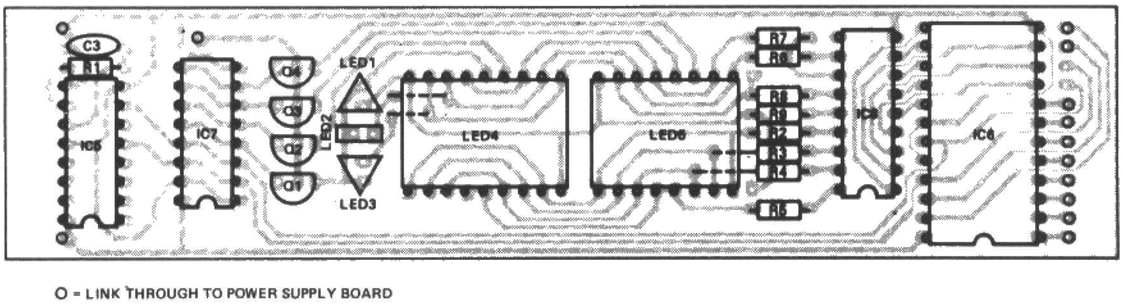


Fig. 7 Component overlay for the display board.

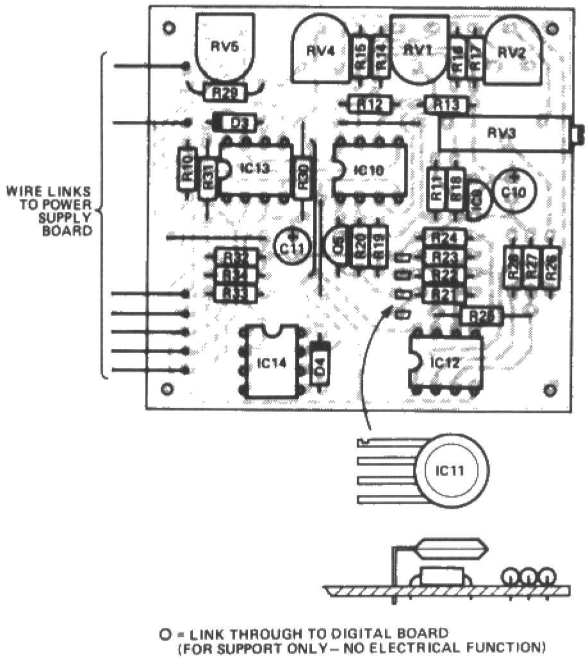


Fig. 8 Component overlay for the analogue board.

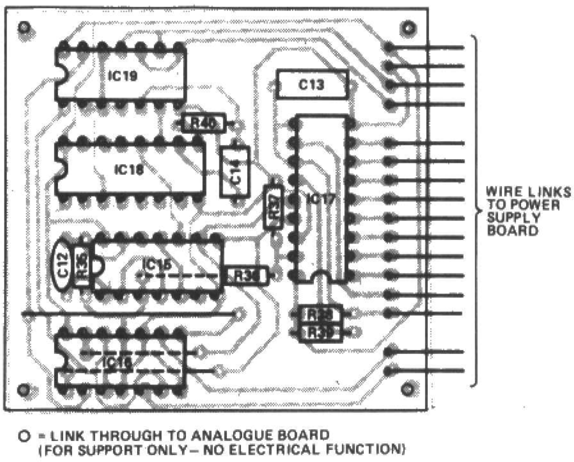


Fig. 9 Component overlay for the digital board.

live tracks are insulated with epoxy resin glue after soldering.

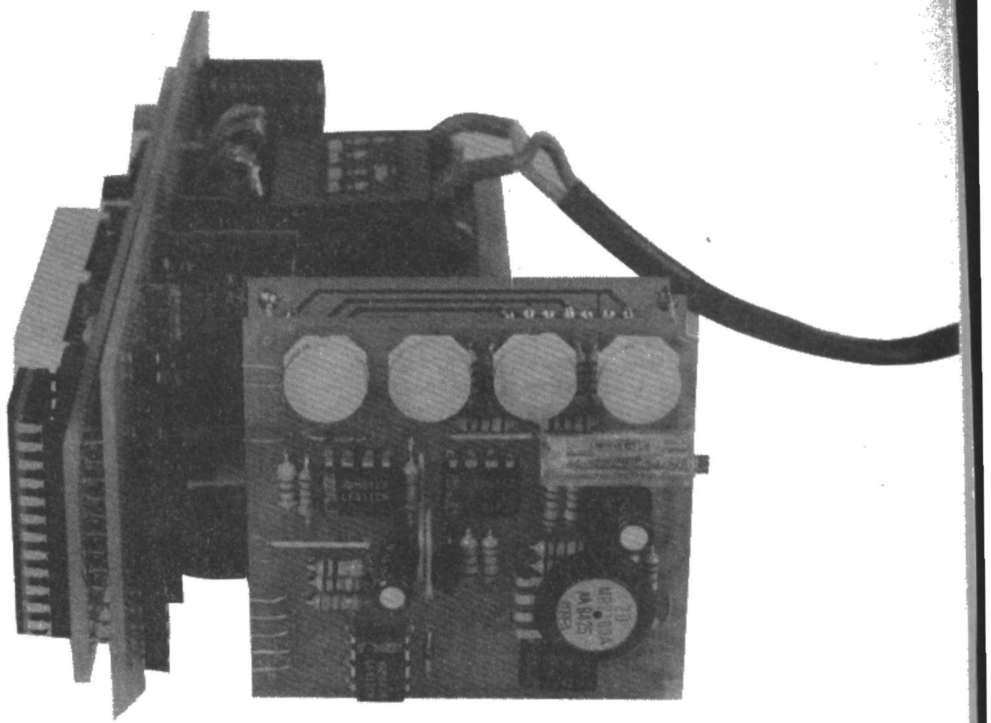
Fit all the components onto the boards, starting with the wire links, then the resistors, capacitors, semiconductors, and finally the bulky parts. Note that some links and resistors are fitted under ICs and the displays, particularly R36 which will need to be a miniature type to squeeze into place. A standard resistor could be used if it is fitted underneath the board.

It is recommended that IC6 and the displays are fitted in sockets. The use of sockets for the other ICs is optional. IC3 requires a small heatsink. The pressure transducer IC11 should have its leads carefully bent with pliers, so that it will fit parallel to the board over resistors R21–28.

Save the cut off legs from the resistors and capacitors, and use them to interconnect the boards. Fit a good length in each of the positions passing off the analogue and digital boards, bent parallel to the surface. Pins should also be fitted to the display board, but not bent this time, standing proud from the rear of the board.

Make the analogue and digital boards up into a module by soldering links into the holes which have been provided in the corners. The components should end up on the outside surfaces, with the boards spaced so that the links line up with the holes on the motherboard. When this has been done, the module can be fitted onto the motherboard and soldered. Trim off any excess from the links. Alternatively, you can use SIL PCB sockets on the motherboard and just push the bent links into them.

Finally, the display board is sandwiched onto the motherboard in much the same way. Some delicate soldering is required here as the fifteen soldered points appear between the panels. Make sure the display board is parallel to the motherboard, and as close as is reasonable without them shorting together.



PARTS LIST

RESISTORS (¼W 5% unless otherwise stated)	
R1	18k
R2-9	100R
R10	4k7
R11	2k7
R12, 13, 15	10k 1% metal film
R14	36k 1% metal film
R16, 17	1k0 1% metal film
R18	6k8 1% metal film
R19	33k 1% metal film
R20	15k 1% metal film
R21, 22	39k 1% metal film
R23, 24, 27, 28	1M0 1% metal film
R25, 26	130k 1% metal film
R29	680R 1% metal film
R30	330k 1% metal film
R31, 33	15k
R32, 34, 39	10k
R35	8M2
R36	47k (see text)
R37	82k
R38	390R
R40	1M8
RV1	5k0 horizontal cermet
RV2, 4	1k0 horizontal cermet
RV3	10k 15-turn cermet
RV5	10k horizontal cermet
CAPACITORS	
C1, 3, 5, 7	47u 25V radial electrolytic
C2, 4, 6, 8-12	10n 5% polycarbonate
C13	220n 5% polycarbonate
C14	390n 5% polycarbonate
SEMICONDUCTORS	
IC1	78L12
IC2	79L05
IC3	78M05
IC4	78L05
IC5	4060
IC6	2732
IC7	4555
IC8	ULN2803A
IC9	LM335Z
IC10, 12	LF412
IC11	MPX100A
IC13, 14	LF411
IC15	4011
IC16	4013
IC17	ZN435
IC18	4060
IC19	4025
Q1-4	2N3706
Q5	BC184L
D1, 2	1N4001
D3, 4	1N4148
BR1	W005
LED1, 3	red triangular LED
LED2	red rectangular LED
LED4	common anode 1½ digit LED display, red
LED5	common anode 2 digit LED display, red
MISCELLANEOUS	
T1	9-0-9V, 500mA mains transformer, chassis or PCB-mounting (see text)

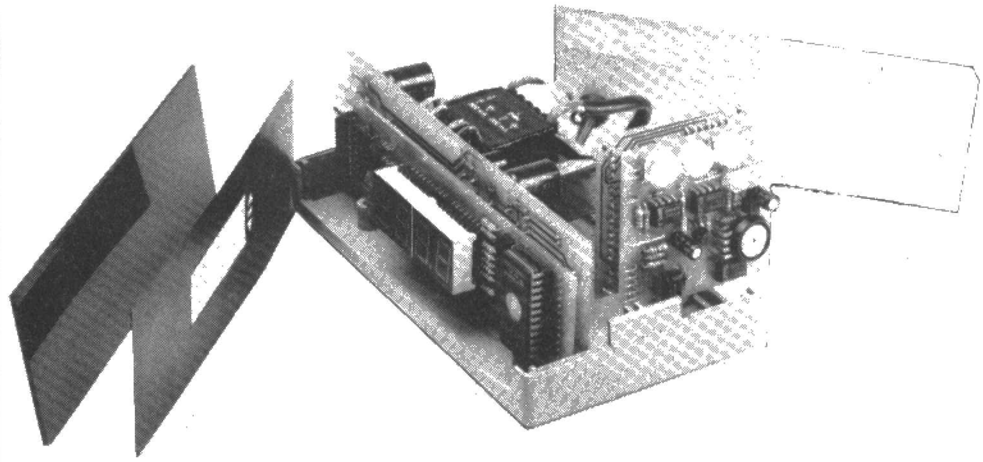
PCBs; case, Vero type 202-21041C; red filter sheet; black plastic sheet; IC sockets; strain relief grommet; mains cable; heatsink.

The display board is designed to accommodate a two digit and a one-and-a-half digit LED, but some trouble was experienced in matching their brightnesses. This can be solved by using a pair of two digit displays and removing pins 16–18 from the one in the most significant position. Cut them as close as possible so that they do not make contact with the socket.

The overall assembly slots into guides moulded into the case. Some ventilation holes are needed in the base and rear panel near the transformer, and a hole in the rear panel is required for the altitude adjustment screw (on RV3). Once everything is fitted into the case the screw will sit flush in the hole.

Fit a strain relief grommet where the mains lead passes through the rear panel. Some notches will be needed in the case moulding to accept the end of the analogue and digital module.

To finish off, the aluminium front panel of the box is discarded and replaced with a piece of red display filter (see Buylines), and, to make a really neat job, a mask is cut from a piece of black plastic or card and slipped over the LEDs to hide the circuitry from view.



Testing And Calibration

Set all the preset resistors to their central positions, short out R30, and switch on. The display should show something, most probably 'ur' which indicates under-range. Four dots mean an illegal code on the trend sense lines, in which case the connections should be checked.

The display may begin counting up from 845. This is normal because of the way the A/D converter works. Once calibrated, the display will show 'ur' on switch-on, then ramp up to the actual reading and stop. In its uncalibrated state, the display is likely to stay at 'ur', or count up to 1098 and then show 'or' for over-range. When the display shows either under or over-range, the trend indicators are disabled.

It should be possible to make the display show a number by adjusting RV3 — anticlockwise for 'ur' or clockwise for 'or'. If the display will not budge from 'ur', set RV3 fully anticlockwise and switch the unit on and off a few times. Some problems were experienced with the prototype latching up on switch on, but this is not a problem after it has powered up satisfactorily.

Having obtained a numeric display, note carefully how much adjustment of RV3 is needed to change the display from one number to the next, always turning RV3 in the same direction. Maximum noise immunity is set with RV5 by adjusting it so that, having increased the displayed number by one, it only returns to its previous value by turning RV3 back one-and-a-half times as far.

As an initial set up, RV1 and RV2 may be left in their central positions. However, if a sensitive meter is available, RV2 should be adjusted so that the voltage at its wiper is the same as V ref.

A crude calibration can be achieved over a period of time by watching the TV weather forecasts. Each line on the chart represents 4mb. Watch how the pressure changes and adjust RV4 so that the displayed pressure changes by the same amount. RV3 can then be used to adjust for the overall offset.

Accurate calibration will require an experimental set-up similar to that illustrated in Fig. 10. One millibar of pressure is equivalent to a difference in heights of 10mm in the water level in the manometer tube. Any old tubing can be used for this. I used tubing from a home brew beer kit.

RV1 should be adjusted first. Use a standard pressure change (say 50mb — you will be surprised how hard a blow that is!) and tweak RV1 until the barometer maintains a constant scale factor over a range of temperatures.

Then RV4 can be adjusted so that, for a 50mb blow, the display changes by 50. RV3 is adjusted to bring the display into line with the weather charts. Remove the short from across R30. Any adjustments made now will take several seconds to affect the display. RV3 may need to be trimmed again. Any remaining temperature sensitivity can be trimmed out with RV2. **ETI**

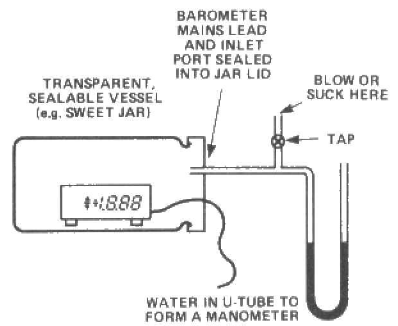


Fig. 10 Arrangement used to calibrate the Digibaro.

BUYLINES

The resistors, capacitors and semiconductors are all widely available with the exception of the MPX100A pressure transducer. There are two companies who should be able to help here, Hawke Electronics of Amotex House, 45 Hanworth Road, Sunbury-on-Thames, Middlesex, tel 01-979 7799, and Macro Marketing, Burnham Lane, Slough SL1 6LN, tel 06286-4422. The display filter used in the prototype came from RS Components, but it shouldn't be too difficult to find other filters which can be cut to size. Most of the other components, including the case, came from Maplin, but there is nothing terribly specialised here and most of the parts should be available from other suppliers too. We do not know of anyone who can supply programmed EPROMs for this project, but a copy of the listing is available in return for an SAE. The PCBs will be available from our PCB Service.

6809-BASED MICROCOMPUTER

Dave Rumball and Gary Mills conclude their description of the workings of the computer before going on to consider the choices facing constructors and the assembly of the two boards.

The real time clock, IC27, is a 146818. This part is designed for a multiplexed processor address/data bus, but here is used with a non-multiplexed processor by means of a separate address decode for the address and data strobes. The CE line is grounded by a transistor which is held on by the main +5V rail. When the system power fails, the chip is disabled in order to prevent corruption of the data. The clock has its own internal oscillator which is driven by a 32.768 kHz crystal to reduce power consumption. Power for the clock is provided by a trickle-charged NiCad battery when the main power is off.

The 146818 also contains 64 bytes of CMOS RAM which are used to hold various system parameters, such as the serial baud rates, video timing parameters etc. An RC network on the PS input gives an indication of battery failure. The software checks for this condition on power up and loads a default set of system parameters if the battery power has failed.

The Display Section

The display section consists of three parts, the NEC7220A graphics controller IC34, a 128K bank of DRAM, ICs47–62 (not part of the processor address space), and some control logic. The NEC7220A does 98% of the work in producing the video. It generates the correct display address for the RAM, master timing strobes for reading and writing to the RAM, and display blanking and synchrony signals. The sixteen bit display address is multiplexed onto the eight bit RAM address by

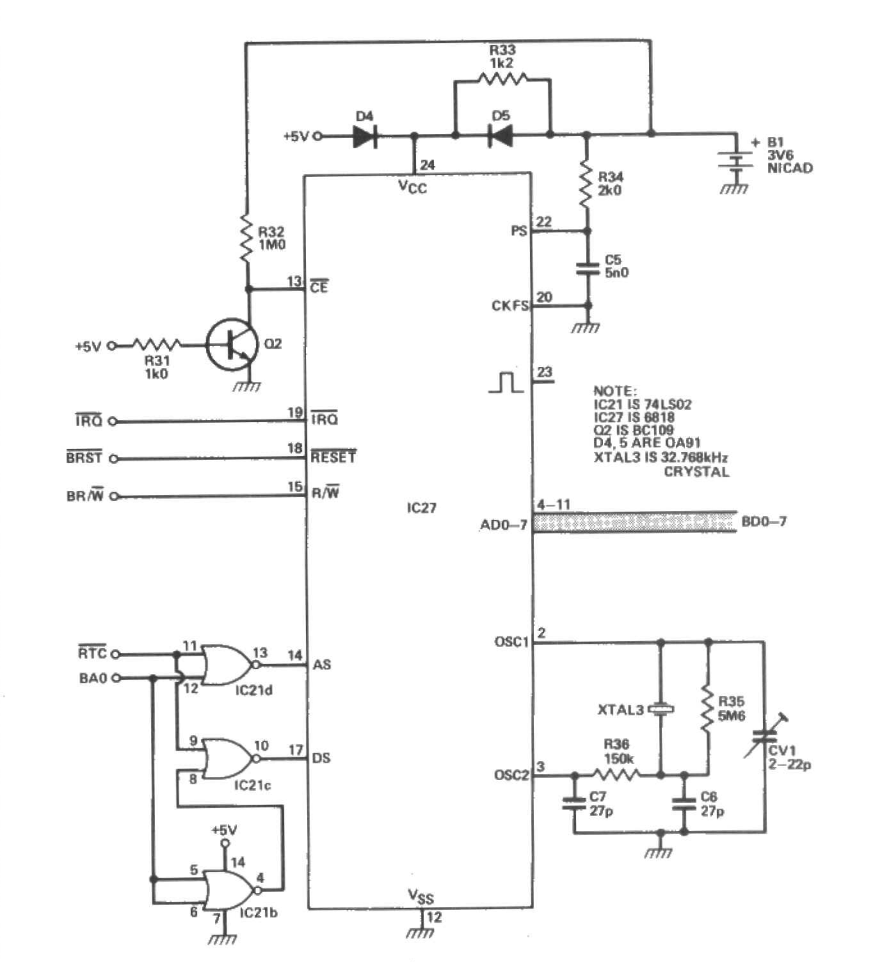


Fig. 1 Circuit diagram of the real time clock.

OOPS!

A capacitor should be added to the serial interface controller oscillator circuit shown in Fig. 4 on page 38 of last month's issue. The capacitor is C30, a 27p polystyrene type, and should be connected between pin 32 of IC20 and the 0V line. It has been included in the overlay diagram and the parts list in this article.

In Fig. 2 on page 37 of the January issue, XTAL1 is listed as a 10MHz crystal. It should be a 16.000MHz crystal, as stated in the parts list in this article.

ERROR NOTED IN ETI JANUARY 1986

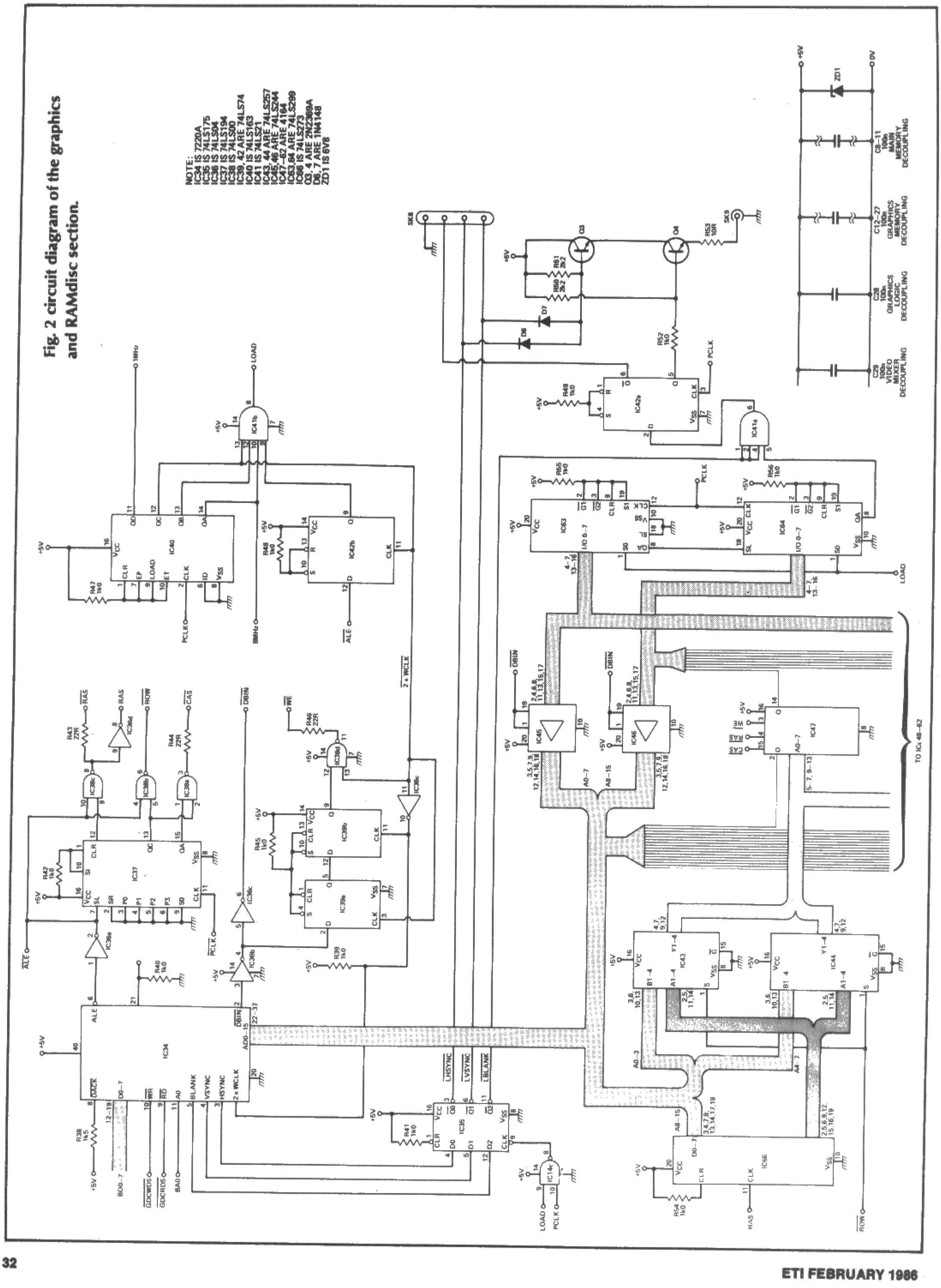


Fig. 2 circuit diagram of the graphics and RAMdisc section.

IC43 and IC44. IC66 latches the low order address lines so that they are stable during the later part of the memory cycle when the graphics controller is putting data onto the address/data bus.

The control strobes for the display DRAM are derived from the master timing signal ALE from the controller. This signal is clocked along a shift register by the pixel clock, to form a digital delay line. Various signals from the shift register are gated to provide the RAS and CAS strobes for the DRAM, and the row select signal for the multiplexer. The WE strobe for the DRAM is derived by delaying the DBIN signal from the graphics. The DBIN signal also gates read data from the DRAM to the controller data lines via tristate buffers IC45 and IC46. Note that the graphics controller data bus is sixteen bits wide.

The graphics controller draws by using a 'read-modify-write' cycle. First the draw address is output, then the data from that word of memory is read into the controller, modified according to the particular pixel to be plotted, and in the same memory cycle, written back into the RAM. Thus, even though the controller only draws one pixel at a time, it operates only on sixteen bit words. Every sixteen pixel times, data from the DRAMs is loaded into two shift registers IC63 and IC64. The load signal is produced by the counter IC40, which generates the graphics controller clock at 2MHz and an 8MHz clock used by the floppy disc controller.

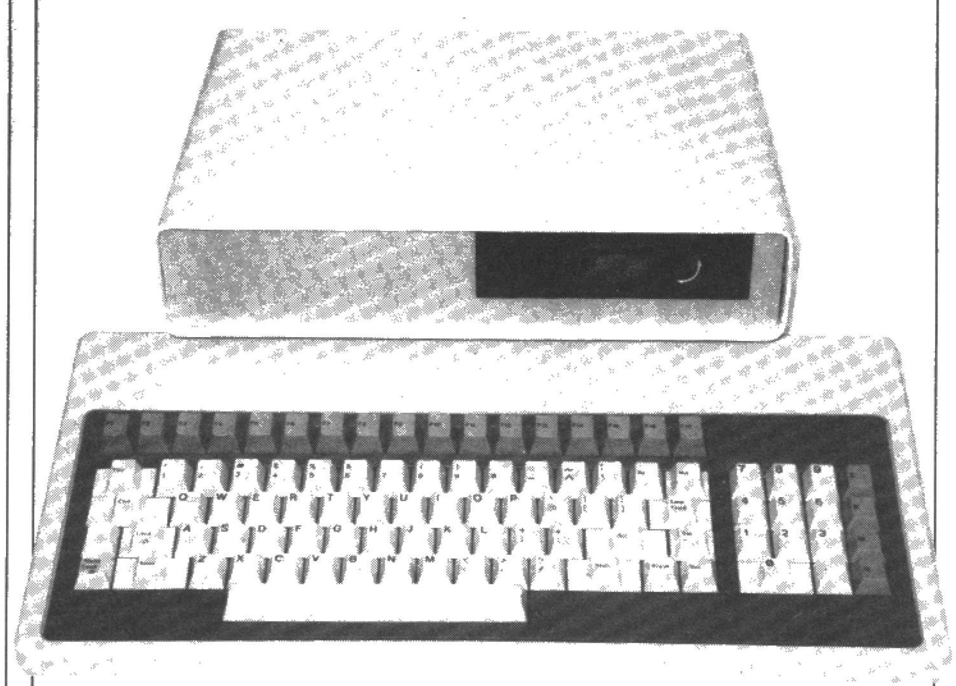
The video data is clocked out at the pixel rate from the shift registers through a blanking gate IC41, and a latch which forces the blanking to a pixel boundary. The resulting video signal is then mixed with the horizontal and vertical syncs and converted to an impedance of 75 ohms by the video buffer. TTL level sync and video signals are also taken out for use with non-standard monitors. The graphics controller is only allowed to access the display memory during line and field blanking times, so there are no flashes on the screen during plotting.

System Choices

The basic kit supplied by Micro Concepts includes the main printed circuit board, the EPROM disc board, a programmed monitor EPROM (IC3), a diskette of system-related software and the necessary documentation. The remaining parts must be obtained from other sources by the constructor.

If cost is an important consideration, construction of certain parts of the system can be left for the time being and only the heart of the system assembled. For example, if serial interfacing is not required, the circuitry associated with the two serial ports can simply be omitted. It is easy enough to add the required components later should the need for a serial interface arise. The following notes should help you decide which components to include and which to omit.

Video output: the board will not function correctly if IC34 is not fitted, but the rest of the graphics circuitry is only required if a video monitor is to be used. If you plan to use the system with a terminal instead, ICs 35, 45, 46, 63, 64 and 47–62 can safely be omitted, along with SK8 and SK9 and the circuitry around Q3 and Q4. However, note that the RAMdisc facility will not function if the memory is not installed.



The 6809-based microcomputer fitted in a Vero case and equipped with a keyboard and 3.5" disc drive. Details of this and other case options will be given next month.

EPROM disc: if this facility is not needed, all of the components on the plug-in board can be omitted (ICs 29–33, RP3 and SK7) along with IC28 and SK6 on the main board.

Floppy disc: ICs 24–26, RP2, R27–30 and SK5 can be omitted if this facility is not required. Note that only the monitor mode is accessible if the board is run without discs.

Serial ports: if the RS232 ports are not needed, ICs 20, 22 and 23 can be omitted along with SK3 and SK4 and the circuitry around XTAL2. This is the only section of the board which uses the plus and minus 12V supplies so, unless these rails are required for a disc drive or other peripheral unit, dispensing with the serial ports will reduce the power supply requirements to a single +5V rail.

A number of other components can be omitted in certain circumstances. SW2 is the on-board reset switch and will only be needed if the board is to be used free-standing (that is, without a case). SK10 is the expansion bus socket and need only be fitted if the expansion bus is to be used. Some or all of the decoupling

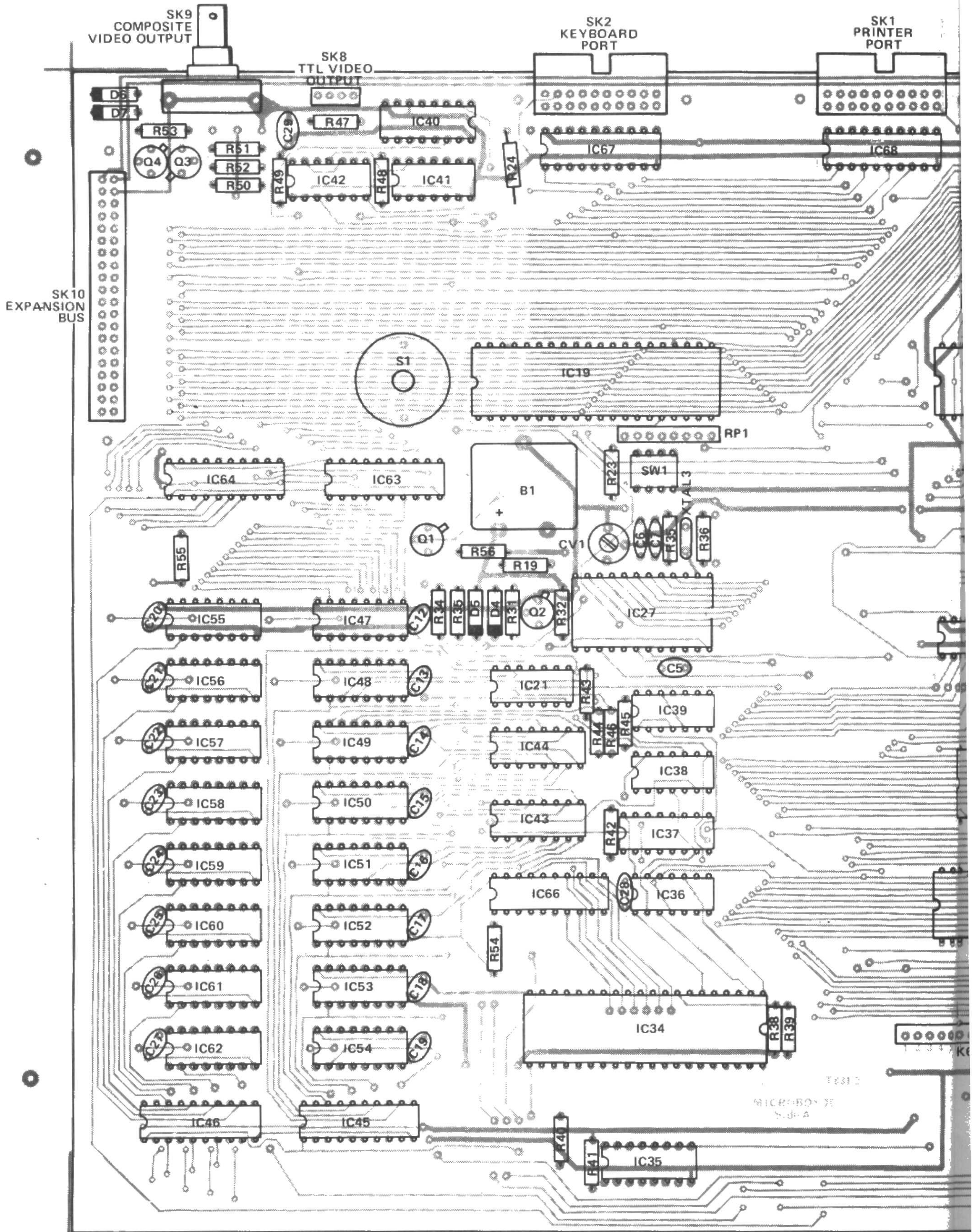
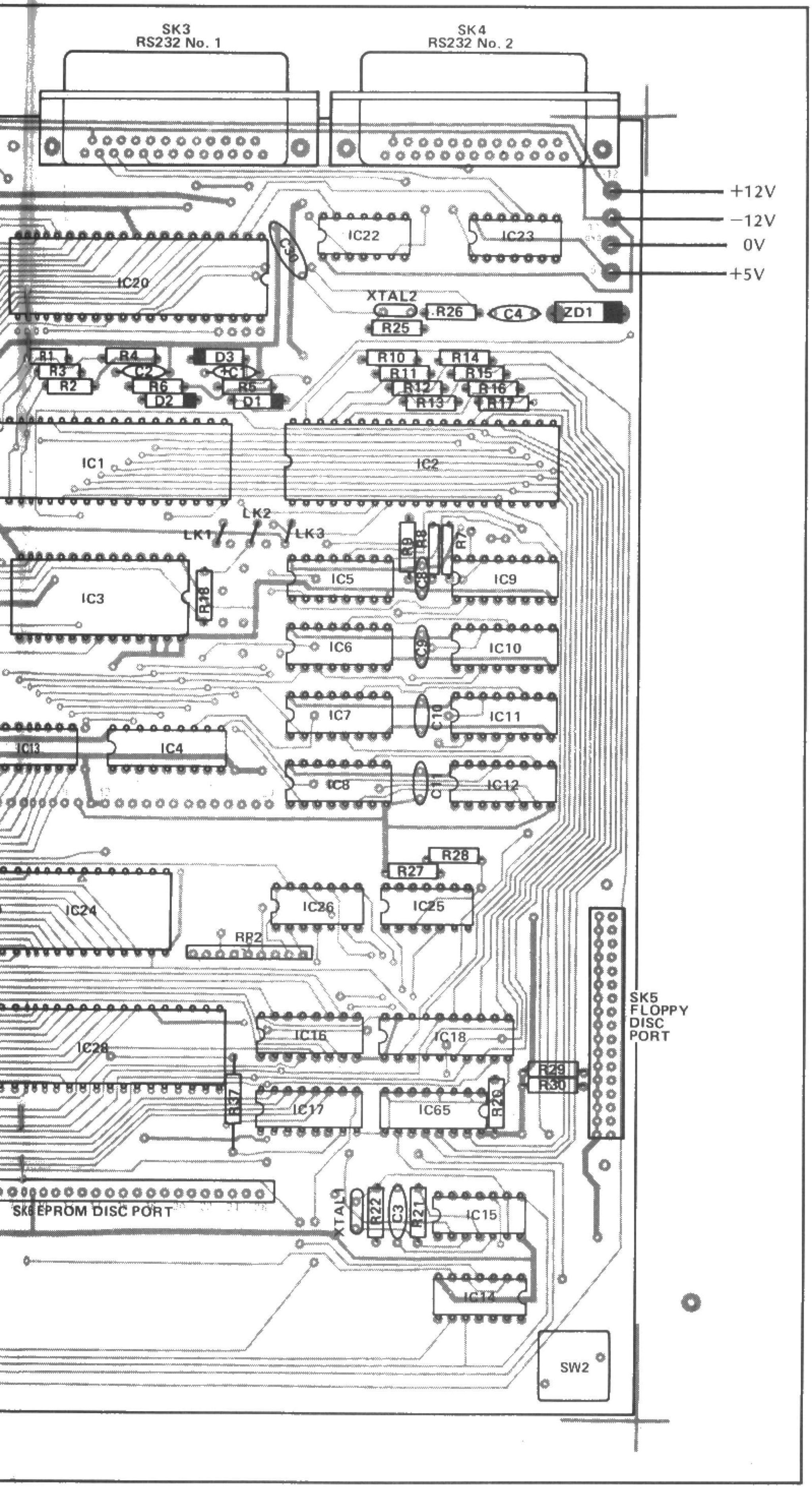


Fig. 3 Component overlay for the main printed circuit board. The board is double-sided but for reasons of clarity the top foil only is shown here.



capacitors around the graphics memory and logic (Cs 12–29) can be left off if this circuitry is to be omitted and of course, IC sockets will not be required for ICs which are not to be fitted.

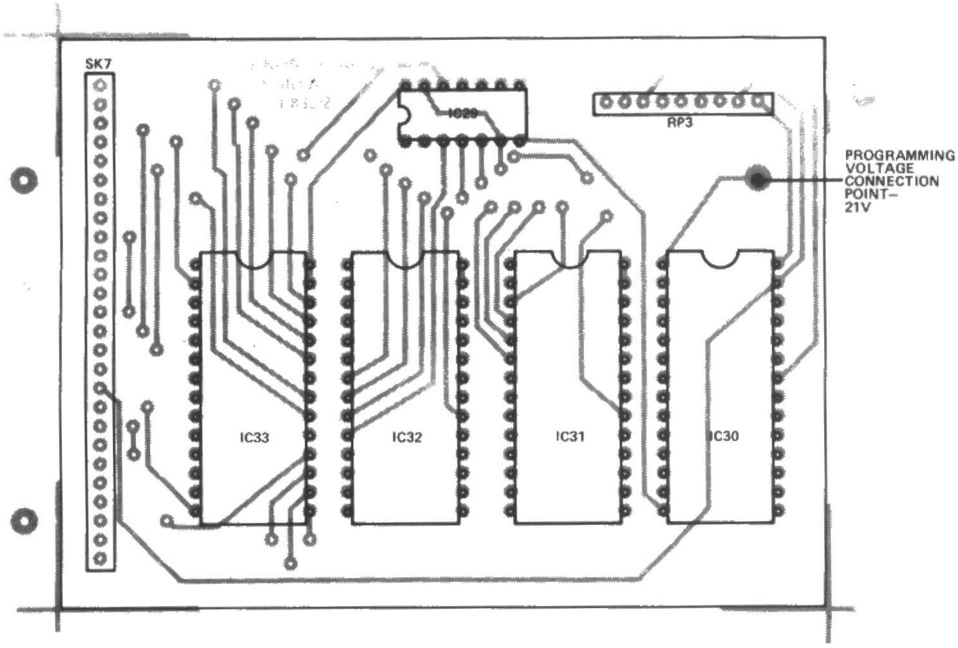
One more thing has to be decided before construction can begin, and that is whether to use straight or right-angled plugs and sockets for the various connections to the board. This will largely depend on the choice of case. Whatever size of case is used, it will probably be most convenient to use right-angle connectors at the rear of the board and poke them directly through holes in the back of the case. It may also be possible to use right-angle connectors for the floppy disc port and expansion bus socket and bring these out directly to the sides of the case. The EPROM disc socket, however, is not adjacent to the edge of the board, and it may be easier to use a straight connector here and punch a slot in the top of the case to provide access. Those who really want to keep costs to a minimum may decide to use the board without a case, thus removing all constraints on the angling of the connectors. One of the prototypes has been working perfectly in this way for some time now, fixed vertically to a wall above the workbench.

Construction

The boards supplied by Micro Concepts are electronically tested for shorted and broken tracks before despatch. However, given the complexity of the board, it is a good idea to examine it carefully against a strong light before starting since any errors which have slipped through will be much more difficult to identify once all the components are in place. It is also a good idea to check that the larger components fit comfortably into their holes. If necessary, the holes can be enlarged slightly with a drill, but bear in mind that this will remove the through-hole plating and make a note to solder carefully on both sides of the board at such points.

Begin by installing the IC sockets. Although most of the ICs have to be inserted with pin 1 towards the left-hand side of the board (the side on which the video outputs and the battery are located), a number of them face in

Fig. 4 Component overlay for the plug-in EPROM disc board. This board is also double-sided and again, only the upper foil is shown.



PARTS LIST

RESISTORS

R1-5	10k
R6	100k
R7-17, 43, 44, 46	22R
R18	68R
R19, 20, 23, 24, 26* 31, 39-42, 45, 47-49, 52*, 54-56	1k0
R21, 22, 27-30*	330R
R25*, 32	1M0
R33	1k2
R34	2k0
R35	5M6
R36	150k
R37	3k9
R38	1k5
R50*, 51*	2k2
R53*	10R
RP1	10k x 7SIL resistor pack
RP2*	1k0 x 7 SIL resistor pack
RP3*	10k x 8 SIL resistor pack

CAPACITORS

C1	47u 6V tantalum
C2	100n 63V polyester
C3	10n polystyrene
C4*	56p polystyrene
C5	5n0 polystyrene
C6, 7, 30*	27p polystyrene
C8-29*	100n ceramic
CV1	2-22p trimmer

SEMICONDUCTORS

IC1	68B09E
IC2	6883
IC3	2764 (monitor EPROM)
IC4	74LS465
IC5-12, 47-62*	4164
IC13	74LS245
IC14, 38	74LS00
IC15	7404
IC16	74LS139
IC17	74LS138
IC18, 45*, 46*, 67, 68	74LS244
IC19	68B21
IC20*	WD2123
IC21	74LS02
IC22*	75188
IC23*	75189
IC24*	WD1770
IC25*	7407
IC26*	7406
IC27	6818
IC28*	8255
IC29*	74LS393
IC30-33*	27128
IC34*	NEC7220A
IC35*	74LS175
IC36	74LS04
IC37	74LS194
IC39, 42	74LS74
IC40	74LS163
IC41	74LS21
IC43, 44	74LS257
IC63*, 64*	72LS299
IC65	74LS85
IC66	74LS273
Q1	BC108
Q2	BC109
Q3, 4	2N2369A
D1-3, 6*, 7*	1N4148
D4, 5	0A91
ZD1	6V8 PN junction voltage transient suppressor

MISCELLANEOUS

B1	3.6V 100mAh PCB-mounting NiCad battery
S1	PCB-mounting piezo-electric sounder
SK1, 2	20-way IDC header plug, straight or right-angle mounting (see text)
SK3*, 4*	25-way D socket, straight or right-angle mounting (see text)
SK5*	36-way IDC header plug, straight or right-angle mounting (see text)
SK6*	26-way PCB header plug, straight or right-angle mounting (see text)
SK7*	26-way PCB header socket
SK8*	4-way PCB header plug, straight or right-angle mounting (see text)
SK9*	PCB-mounting BNC socket
SK10*	40-way IDC header plug, straight or right-angle mounting (see text)
SW1	4-way DIL switch
SW2*	SPST keyboard switch, PCB-mounting
XTAL1	16.000MHz crystal
XTAL2*	1.843 MHz crystal
XTAL3	32.768 kHz crystal

PCB; IC sockets*: 13 off 14 pin DIL, 32 off 16 pin DIL, 10 off 20 pin DIL, 1 off 24 pin DIL, 6 off 28 pin DIL and 6 off 40 pin DIL; case; power supply.

* These components may be omitted under certain circumstances — see text.

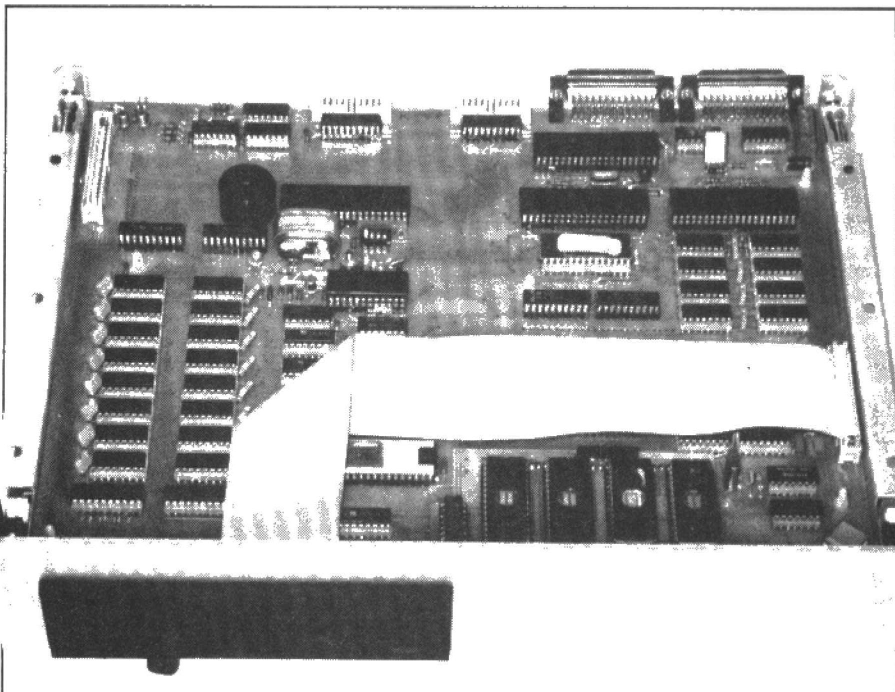
the opposite direction. Check carefully against the overlay diagram as you work and check again afterwards just to make sure. When all the sockets are in place, check each one carefully for solder splashes between pins, bad joints and so on.

Continue with the assembly by installing the three wire links, the various input and output sockets, the switches, the piezo-sounder, the resistors and the capacitors. Make sure that you install the tantalum capacitor, C1, and the three resistor packs the right way around. Solder the diodes and transistors into place, again taking care that they are the right way around, but do not insert the ICs or the Nicad battery. Finally, install the three crystals.

Now comes the tedious bit! Visually check the board for solder bridges and missed joints, then check again that every component is in the right place and that the critical components are all the correct way around. Using a multimeter, carefully check the following buses for continuity and for short circuits between adjacent lines:

the address lines between the CPU (IC1), the SAM (IC2) and the EPROM (IC3);

the data lines between the CPU (IC1), the EPROM (IC3) and the buffers (IC4 and IC13);



Another view of the cased board. Note that the EPROM disc board shown here (lower centre-right) is a prototype.

the data lines between the buffers (IC13) and the various peripheral device controllers (ICs 19, 20, 24, 27 and 34);

the address and data lines between the controllers and their associated circuitry (eg., between IC19 and the buffers IC67 and IC68);

the main (64K) RAM address lines;

the graphics (128K) RAM address lines.

Connect up a supply of +5V to the board and check that the IC sockets all have +5V and 0V appearing on the correct pins. Repeat the procedure with the +12V and −12V rails. If all is well, insert the ICs into their sockets, taking great care that each IC is in the correct socket and the right way around.

Construction of the plug-in EPROM disc board should present no problems at all, but again, it is a good idea to check the bare PCB before starting and the usual care should be taken with the orientation of the resistor pack and the ICs. One refinement worth considering here is the use of a ZIF (zero insertion force) socket in the IC30 position. This is the position in which EPROMs can be programmed, and the additional cost of a ZIF socket may well be justified if you plan to make extensive use of this facility.

● Next month's article will cover the choice of case, power supply, keyboard and monitor for use with the board and the testing and setting up of the system.

ETI

BUYLINES

Almost all of the integrated circuits are available from Technomatic, but there are a number of exceptions. The WD2123 and WD1770 (IC20 and IC24) are available from Pronto Electronics Systems Ltd, 466–478 Cranbrook Road, Gants Hill, Ilford, Essex IG2 6LE, tel 01-554 6222. Pronto currently offer the two chips together at a discount (the WD2123 is very expensive) and you should contact them for details. Note that there are two versions of the disc controller, the WD1770 which supports stepping rates from 6 to 30ms and the WD1772 which supports stepping rates from 2 to 6ms. Both versions will work on this board. Pronto can also supply the 68B09E (IC1) and the 68B21 (IC19).

The NEC7220a graphics controller chip is available from Semi Components Ltd, Vine House, 104 Ashley Road, Walton-on-Thames, Surrey KT12 1HP, tel 0932-241866. There are two versions of this chip, the 7220 and the 7220A. Only the 7220A will work in this design. The MC6883 SAM chip (IC2) can be obtained from Jermyn Distribution Ltd, Vestry Estate, Sevenoaks, Kent, tel 0732-450144. Note that this device is also known as the 74LS783. The transient suppressor ZD1 is an RS part, stock number 283-255. RS Components will only supply to trade and professional customers but Crewe-Allan & Company of 51 Scrutton Street, London EC2 or Trilogic Ltd of 29 Holm Lane, Bradford, will obtain parts from them on payment of a small handling charge.

The resistors and capacitors are all widely available from our advertisers and the usual mail order suppliers. Eight-resistor SIL packs are easy to obtain but seven-resistor ones are not. You can either obtain them from RS via one of the suppliers mentioned above or use eight-resistor packs and cut off one pin. The 2-22p trimmer is also an RS part but similar devices from other suppliers should prove suitable provided their pin-out matches the holes in the board. The same applies to the 3.6V NiCad battery. The basic kit, which includes the PCBs and IC3, is sold by Micro Concepts, 2 St Stephens Road, Cheltenham, Gloucestershire GL51 5AA, tel 0242 – 510525. The PCBs will not be available from our PCB Service.

ETI MICROAMP

Need a lot of audio power in a small space? Then read on as Allan Bradford of Time Machine Sound Engineering introduces the Microamp — a MOSFET amp with the power to deliver 75W RMS.

Despite its small size, the Microamp is crammed with useful features and will deliver powers comfortably in excess of 26W rms per channel into 8 ohms and has a sensitivity of -10dBm for full output. It will also operate in bridge mode as a mono amplifier, in which case the bridge mode output will deliver up to 75W RMS into 8 ohms with a sensitivity of -10dBm for full output. A headphone socket is provided which will deliver equal power into either 8 ohm or 400 ohm professional headphones.

The Start Of Something Small

The Microamp is housed in the standard 1U x 8½" x 6" case (although the heatsink on the back makes the depth 7" overall), and is configured as two separate channels with a crosstalk of -55dB. It can be used as a domestic hi-fi amplifier (in conjunction with a suitable pre-amp); as a monitor amplifier or headphone amplifier for domestic or studio use (particularly for monitoring in home recording studios); and as the heart of talkback, public address or keyboard amplification systems.

Toroidal transformer and steel enclosure keep radiated hum fields to a minimum and promote cool operation with high efficiency. Ample heat sinking is provided and the MOSFETS used are rated at more than twice the power they are expected to handle. They will run cool even at full continuous output and will have a long life. Thermal protection is inherent to MOSFETS, which unlike bipolar transistors have a negative temperature coefficient and are not subject to thermal runaway.

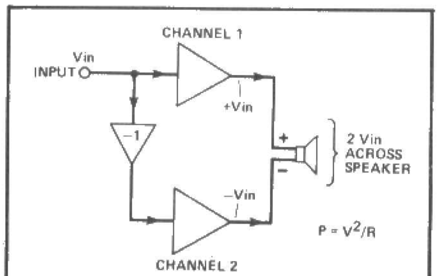


Fig. 1 Bridge mode amplification.

Jack inputs which will accept blanced lines, and XLR outputs meet professional standards. A separate bridge mode output socket is provided.

A Bridge Too Far?

In bridge mode, the input signal to channel 1 is inverted and fed to channel 2 (Fig. 1). The speaker output is then taken between the two channel outputs (instead of between output and ground), so the voltage across the loudspeaker is doubled. Since output power is proportional to the square of this voltage, we can in theory quadruple the power available. In practice, we are limited by the VA rating of the transformer used (the largest that will fit the case). It will give up on us and start to clip the output at around 75W RMS. Even so, this is enough power for most purposes and with an efficient speaker sounds VERY LOUD!

The Microamp is put into bridge mode by turning the channel 2 level control fully anticlockwise until it clicks. At this point the 'on' LED 3 will change from green to red. The channel 1 level control now acts as the volume control for the whole amplifier. Input 1 is the bridge mode input socket.

Clip, Clip, Hooray!

Rather than measure the voltage between output and ground, the 'true clip' indication circuits used in the Microamp measure the difference between the outputs and the supply rails, illuminating LEDs when this becomes too small. At the same time the soft clip facility operates by increasing the negative feedback around the amplifier so as to compress the output. The resulting distortion, should it occur, is much less drastic than that of straightforward clipping and may be compared favourably with the warmer sounding distortion of valve amplifiers (Fig. 2).

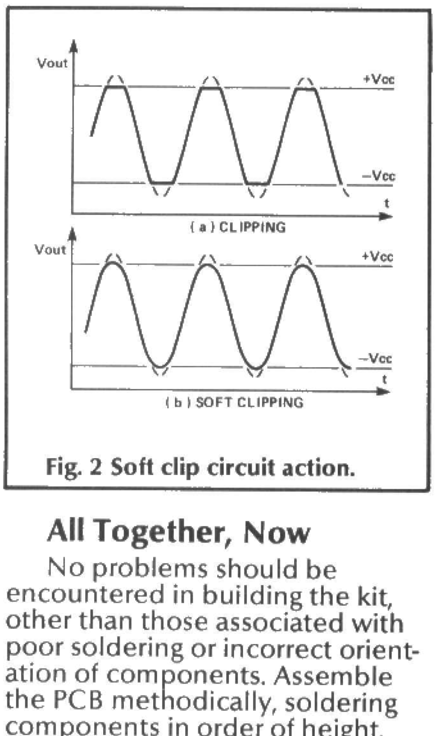


Fig. 2 Soft clip circuit action.

All Together, Now

No problems should be encountered in building the kit, other than those associated with poor soldering or incorrect orientation of components. Assemble the PCB methodically, soldering components in order of height. Leave the large power supply electrolytics to last or they will get in the way. Everything is on this board except for the sockets, transformer, mains switch and fuses. Providing the circuit board is built correctly there is little else to go wrong!

The off-board connections are shown in Figs. 4 and 5. A PCB-mounting terminal block is used to simplify connections to the transformer and output sockets. LEDs are soldered with the bends 5mm above the PCB.

Some of the wire links on the PCB should be made using heavy gauge wire, as indicated.

The MOSFETs should be mounted on the right-angled heat sink bracket using the insulating kits provided (Fig. 6). Both sides of the mica washers should be smeared with a thin layer of silicone

HOW IT WORKS

Line level inputs are debalanced by IC3b and c, configured as unity gain differential amplifiers (Fig. 3). If a mono jack is inserted the inverting input is grounded and each op-amp then acts as a unity gain, non-inverting unipolar amplifier. IC3a inverts the channel 1 signal in order to drive channel 2 when the unit is in bridge mode. The change over is effected by the switch on the back of level 2 pot, RV2, which also changes the colour of LED 3 from green to red.

The power supply is completely standard. C20 and C21 are the main reservoir capacitors and have a ripple current rating of 4A at 100Hz. They will be charged to 60V at 4700µF and should be treated with respect. Discharge them with resistors rather than screwdrivers! The op-amps must of course be run from a lower voltage than the main amplifiers. Since this design is meant to have no hum, monolithic regulators have been employed to provide plus and minus 15V (IC1 and IC2).

It's a wonder anyone still makes bipolar amplifiers now we have MOSFETs with their negative temperature coefficient, very high gate impedance, very low source impedance and ultrafast operation. They allow us to use the simple circuit shown. The whole thing behaves like a large op-amp with a gain of 22 set by R16 (R41). The incoming signal is subjected to two stages of differential voltage amplification — Q1 (Q8) and Q2 (Q9), the Q4 (Q11) and Q5 (Q12) — with the collector output of the second stage being fed by constant current source Q3 (Q10) set to around 15mA. Thsi low noise, high gain, class-A amplifier drives the MOSFET output stages Q6 and Q7 (Q13 and Q14), which are connected as complementary source follower pairs. A more hefty threshold voltage is needed to turn on the gates of the particular MOSFETs we are using (which are chosen for their smallness, hence the unusually high value of PR1 and PR2).

MOSFETs are much faster than bipolars but this makes them more susceptible to high frequency instability. High frequency decoupling is provided around the circuit as a whole with low value capacitors. R18 and C9 (R43 and C19) form a Zobel network to further damp out high frequency instability.

ZD1, ZD2, D2, D3 and R15 (ZD3, ZD4, D5 and D6 and R40) provide the soft clipping. Once the output, either positive or negative going, exceeds the zener voltage, additional feedback is introduced (using the op-amp like properties of the overall circuit) to lower the gain.

IC3d and IC4 compare the output voltages with the supply-rail voltages so that when the output exceeds 82% of the rail voltage, the LEDs start to turn on, indicating the onset of clipping.

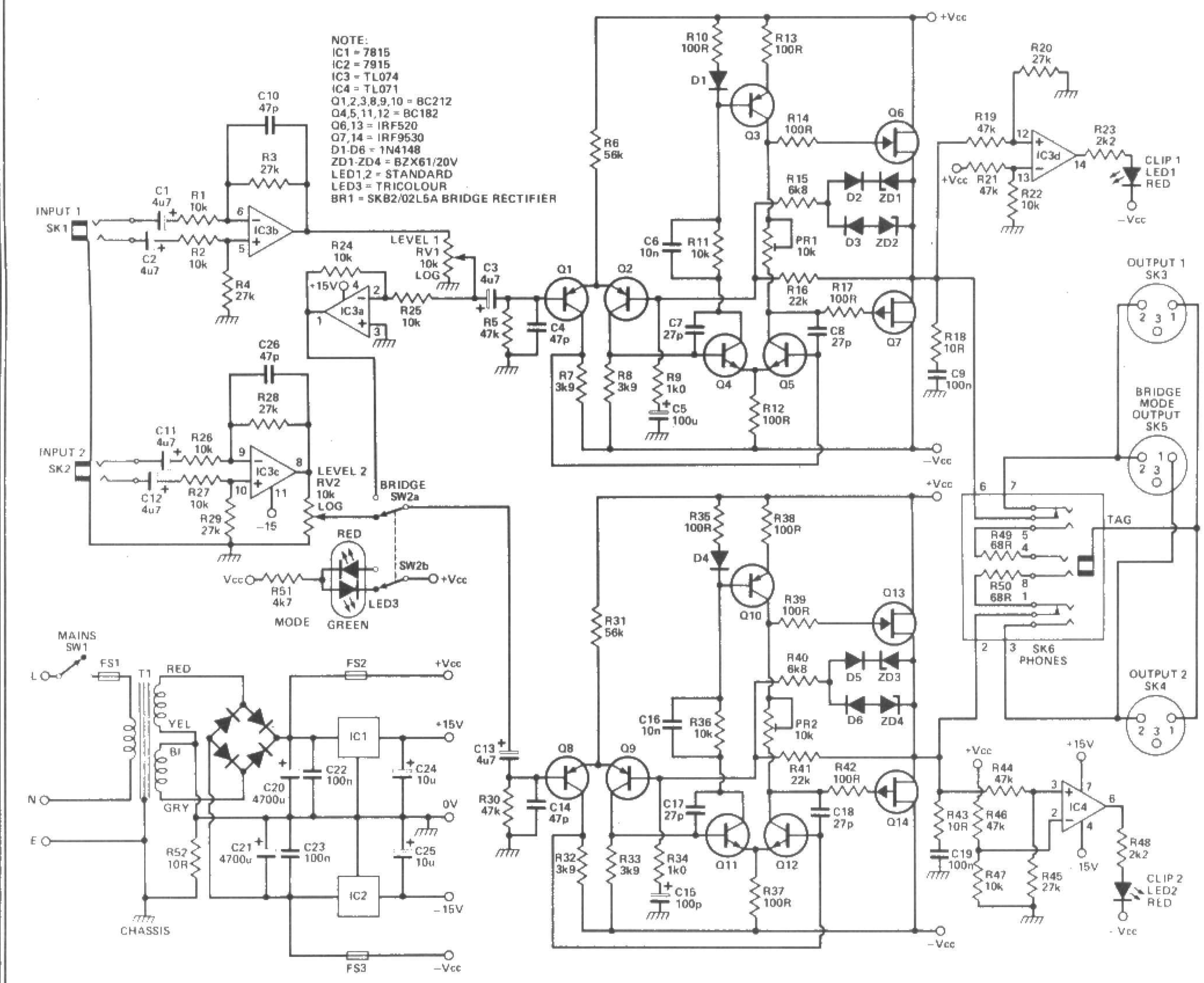


Fig. 3 The complete circuit diagram of the Microamp.

heatsink compound such as 'Thermpath' prior to assembly. Both the back of the right angle bracket and the mounting face of the heatsink should also be smeared with the silicone grease.

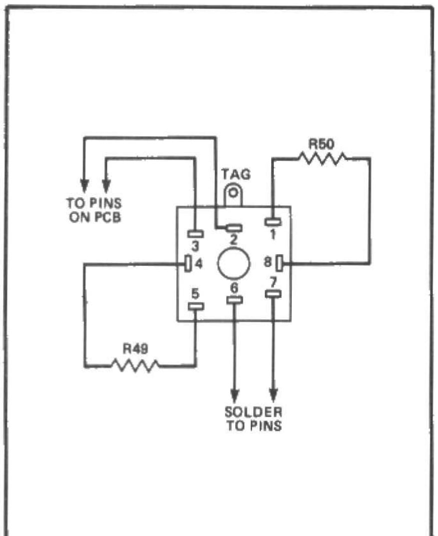


Fig. 4 Headphone socket connections from rear.

The front of the board is held in place in the case by the pots (whose spindles should be cut to 10mm) and the headphone socket. Final assembly is completed by passing the two bolts, with spring washers, through the holes in the back of the right angle bracket and the case, then screwing them into the tapped holes in the heatsink. The wiring may then be completed, ensuring that the insulating boots are pushed over the mains connections to the fuseholder and mains switch.

Setting Up

The only setting up required is to adjust presets, PR1 and PR2. These set the quiescent current in each amplifier, ensuring sufficient current to discharge the gate-source capacitance of the MOSFETs at all frequencies and to bias their gates. This eliminates crossover distortion. Pins are provided on the PCB with wire links enabling an ammeter to be inserted into the positive supply rail to each amplifier (red lead to + ve). Starting with the relevant preset fully anti-clockwise, advance it until the meter reads 15mA. Repeat for the other channel, then solder in the links (switch off first!)

This setting up is not critical. If no ammeter is available, just set the presets not quite fully clockwise. If no distortion is audible, particularly at low volumes, this will probably be good enough.

Use

The Microamp should perform spectacuarly well in all applications. It *will* drive 4 ohm speakers, but remember that no additional power will be available. Clipping will occur at the same power as with 8 ohms speakers.

As with all amplifiers, if you are changing signal source, or changing from -10dBm to 0dBm level signals, or switching to bridge mode, always turn the volume controls down for the sake of your speakers. They will not take kindly to being fed large amplitude square waves.

It is worth mentioning one criticism sometimes levelled at MOSFET amps; their alleged poor bass response. Assuming adequate power is available at bass frequencies, this supposed effect is likely to be psychoacoustic in origin. The excellent transient response of MOSFET amplifiers renders their sound extremely 'transparent'. The resulting improved clarity in the upper registers can actually reveal detail in bass signals, removing the sort of muddiness which is sometimes mistaken for 'extra' bass!

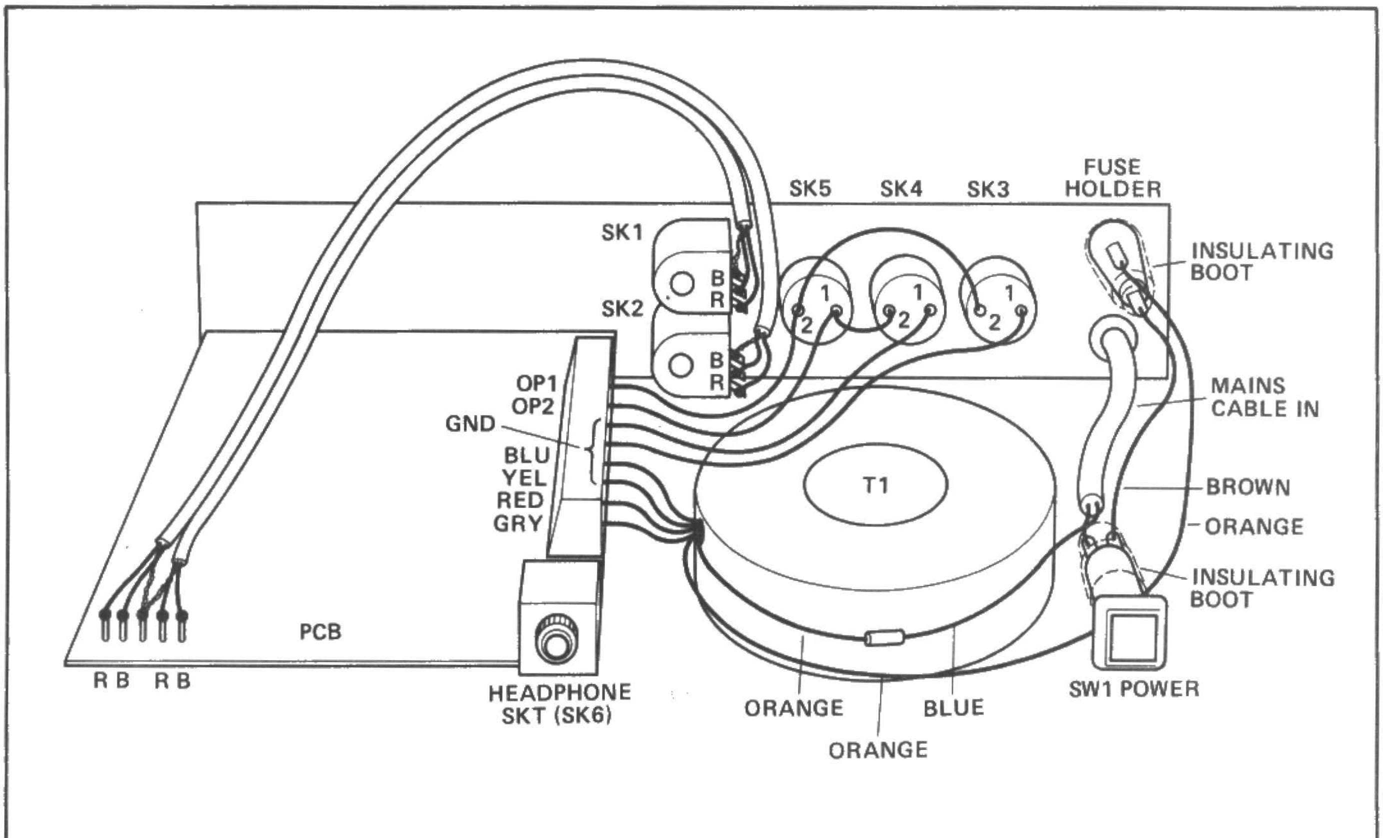


Fig. 5 Off-board connections within the case.

PARTS LIST

RESISTORS (all ¼W, 1% metal oxide unless stated)

R1, 2, 11, 22, 24, 25, 26, 27, 36, 47	10k
R3, 4, 20, 28, 29, 47	27k
R5, 19, 21, 30, 44, 46	47k
R6, 31	56k
R7, 8, 32, 33	3k9
R9, 34	1k0
R10, 12, 13, 14, 17, 35, 37, 38, 39, 42	100R
R15, 40	6k8
R16, 41	22k
R18, 43, 52*	10R
R23, 48	2k2
R49, 50*	68R
R51*	4k7
RV1	10k log pot
RV2	10k log pot with DPDT switch
PR1, 2	10k horiz preset

(* ½W, 5%)

CAPACITORS

C1, 2, 3, 11, 12, 13	4μ7 40V minelect
C4, 10, 14, 26	47p ceramic
C5, 15	100μ 40V minelect
C6, 16	10n polyester
C7, 8, 17, 18	27p ceramic
C9, 19, 22, 23	100n polyester
C20, 21	4700μ 50V axial
C24, 25	10μ 40V minelect

SEMICONDUCTORS

IC1	78L15
IC2	79L15
IC3	TL074
IC4	TL071
Q1, 2, 3, 8, 9, 10	BC212L
Q4, 5, 11, 12	BC182L
Q6, 13	IRF520
Q7, 14	IRF9530
D1-D6	1N4148
ZD1-ZD4	BZX61/20V zener
LED1, 2	red LED
LED 3	Tricolour round LED
BR1	SKB2/02L5A in-line bridge rectifier

MISCELLANEOUS

FS1	20mm, 1A anti-surge mains fuse
FS2, 3	20mm, 2.5 A quick blow fuse
SK1, 2	Stereo ¼" jack skt
SK3, 4, 5	Male panel mtg XLR
SK6	DPDT ¼" jack skt
T1	22+22V, 80VA toroidal mains transformer

Knobs (collet or grub screw, 2 off); PCB; case; heatsink type 1.5E-20; heatsink bracket; 4-way PCB mtg screw terminals (2 off); T0220 mtg kits (4 off); silicone heatsink compount; Veropins (12 off); panel mtg fuseholder, 20mm (1 off); 6BA nuts, bolts and locking washers (6 off); stick-on cabinet feet (4 off); self tap screws (no 4 x 6mm, 4 off); 8-pin DIL skt (1 off); 14-pin DIL skt (1 off).

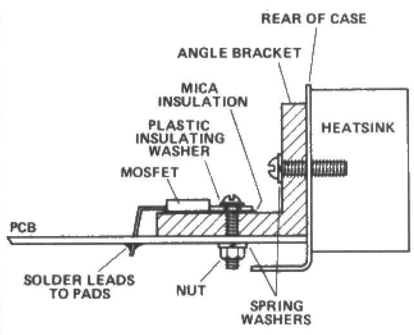
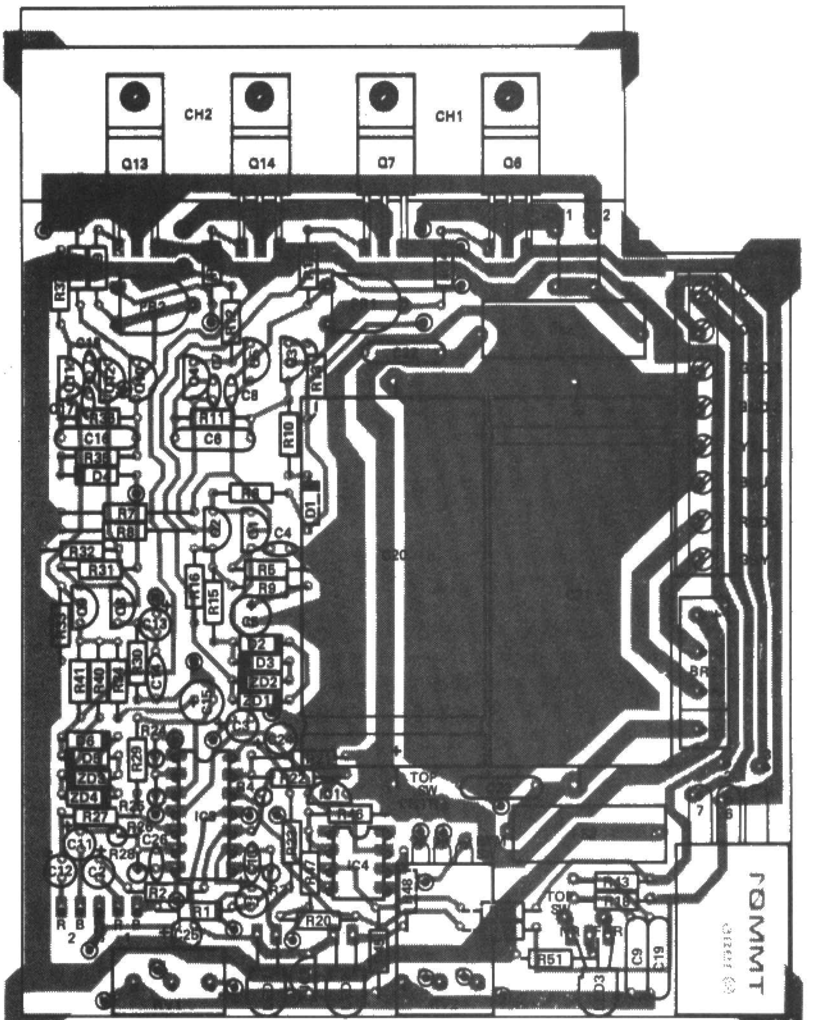


Fig. 6 The assembly of MOSFET, PCB, bracket and heatsink.

BUYLINES

The DPST jack socket is available from Maplin, PO Box 3, Rayleigh, Essex SS6 8LR (0702-554155) as are the zener diodes and the toroidal transformer. The transformer can also be obtained from ILP Electronics, Dept. 9, Graham Bell House, Roper Close, Canterbury, Kent CT2 7EP (0227-454778). The bridge rectifier and the MOSFETs can be ordered from RS through Crewe-Allan, 51 Scrutton St., London EC2 or any supplier who maintains an account with them.

A complete kit of parts including the fully finished steel case and associated hardware is available from Time Machine Sound Engineering for £86.00 including VAT, postage and packing. The legended PCB is available separately at £9.00, the case at £14.00, the heatsink and bracket at £5.00 and the MOSFETs at £12.00 per pair. All prices include VAT, post and packing. Contact:
TIME MACHINE Sound Engineering, Abbotsford, Deer Park Avenue, Teignmouth, Devon, TQ14 9LJ. Telephone 06267 2353.



FLATS ON LEDS TO THE LEFT HAND SIDE

Fig. 7 Component overlay

ETI

DIGITAL SOUND SAMPLER

Paul Chappell describes the keyboard interface and digital control circuitry for the sound sampler.

To complete the analogue circuitry for the sound sampler we need some means of accepting a 1V per octave signal from the keyboard and using it to control the pitch of the note being played. In the first instance, our concern is to get the keyboard signal into the computer's memory. This is achieved by the circuit shown in Fig. 1.

The digital control circuitry is shown in Fig. 2. Most of it is concerned with generating the correct replay frequencies so that the sampled sound is heard at the right pitch. The remainder of the circuit interfaces with the Spectrum and corrects timing errors introduced by delays in entering interrupt service routines. The various control signals for the analogue board are also generated by this circuitry.

HOW IT WORKS

DIGITAL CONTROLLER

IC1 is an oscillator which produces a 2MHz clock. This is divided down by IC2 into the correct frequency relationships for one octave of the equal tempered musical scale. The required note within the octave is selected by IC3 according to the digital code present at pins 11, 13, 14 and 15. This code is supplied by the computer via IC8 and IC9.

The phase locked loop, IC4, and dividers IC5, IC6 and IC7 produce multiples of the selected frequency for the various octave ranges, the particular octave required being selected by the computer via IC8 and IC10. The output from IC10 is used to clock the mobile filters at a rate depending on the selected note.

IC11, IC12 and IC13 generate 'start conversion' (SCS) signals to the ADC at a rate depending on the selected note. When sampling, this will be the sample rate. The analogue board acknowledges receipt of SCS by taking the 'conversion complete' (SCC) line high. This turns off the clock to the mobile filters via IC21a so that the input filter can perform its sample and hold function. The signal also clears down IC12b ready for the next conversion.

When SCC goes low again at the end of the conversion process, the filter clock is allowed to restart, and at the same time IC22a is clocked, putting out an interrupt request (INT) to the computer. In sample mode, the interrupt service routine will read the output of the DAC from the data lines. In replay mode it will write the next digital output onto the data lines to be picked up by the DAC. IC22 is reset as soon as the computer has acknowledged the interrupt request.

The decision about whether to sample, playback, edit the sampled waveform (in software) or wait for a sound trigger is taken by the control register IC14 and IC15. These are accessed by the computer in a normal I/O instruction. The keyboard ADC and pitch selection registers are accessed in a similar way. IC13, IC16, IC17 and associated gates all perform address decoding and timing functions for the input and output. IC23 and IC24 provide vectors for the interrupt routines.

KEYBOARD INTERFACE

The output from a 1V per octave keyboard must be compressed to allow the full six octave span of the sampler to be accommodated within the 2.5V input range of the ADC. The software allows three digital codes for each note, so a little calculation shows that this allows about 30mv per semitone or 360mV per octave. The compression is set by RV5 which controls the gain of IC20.

The keyboard may also produce negative voltages, which must be shifted so that the output from IC21 always lies within the range 0 to 2.5V. The level shifting is provided by RV4, which effectively acts as a tuning control.

IC22 performs the A-to-D conversion of the control voltage. As three adjacent codes are allowed for each note, the aim is to set RV5 so that the middle code is produced. This allows a certain amount of drift in the control voltage without producing the wrong note.

The keyboard gate signal is level shifted by Q2. The input is assumed to be +5V when a key is pressed and 0V otherwise. This is shifted by Q1 to suitable voltage levels for controlling the analogue gate Q2.

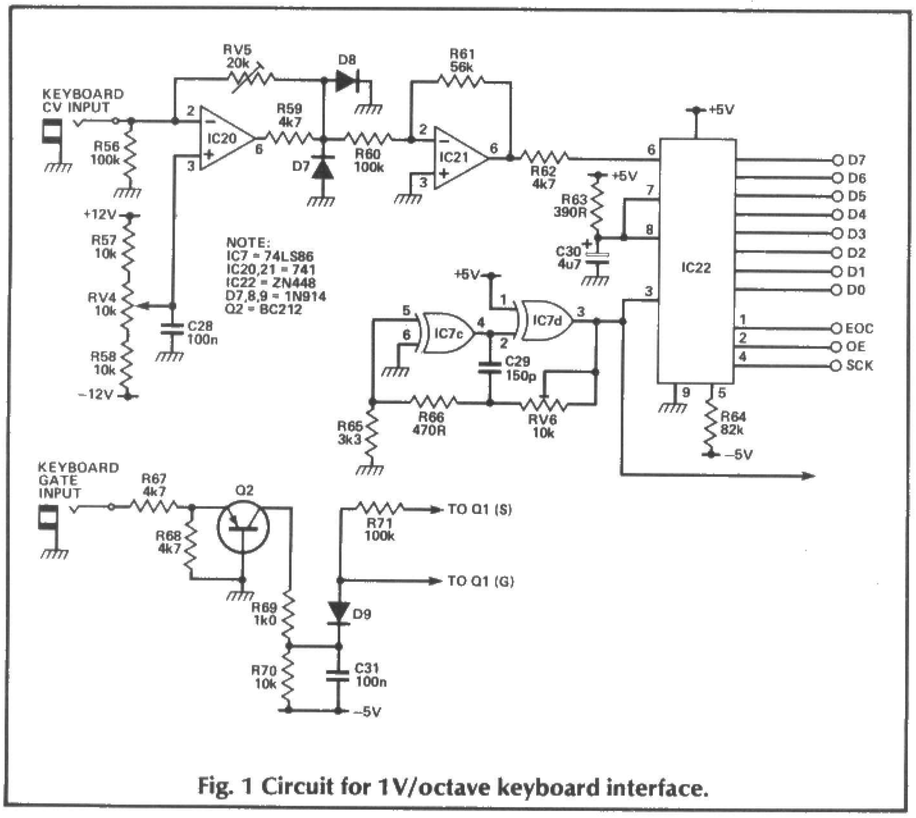


Fig. 1 Circuit for 1V/octave keyboard interface.

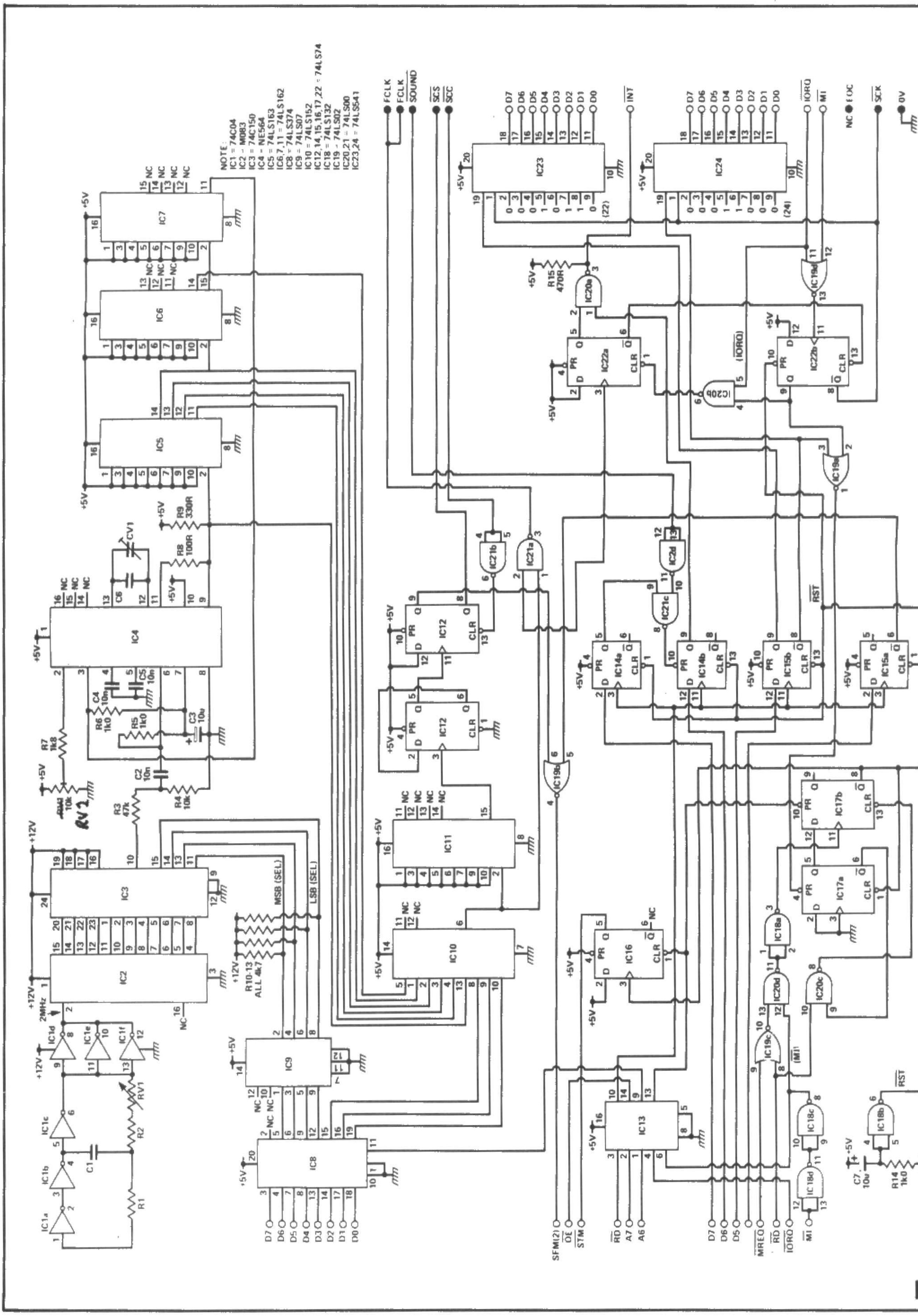


Fig. 2 Digital control circuit of the sampler.

ETI

DIGITAL SUPERGLUE

The superchips of today are beginning to use programmable logic for all the small but vital tasks that hold a complex piece of equipment together. Mike Bedford explores this rapidly developing area before bringing readers an experimental project.

The predominance of VLSI chips in modern computer boards does not mean that small logic devices are becoming a thing of the past. A microprocessor chip does not usually 'bolt' directly into RAMs, EPROMs or PIAs but instead requires a considerable amount of interface logic, using ICs often referred to as 'glue chips' and most frequently being 74LS TTL devices. A look at the inside of many personal computers will confirm that the glue chips often account for a significant proportion of board space. Clearly it would be of considerable advantage if these TTL devices could be combined together into a single integrated circuit. Since each different application has slightly different interfacing requirements the computer manufacturer, rather than the semiconductor manufacturer, would have to specify the device and have it made.

Custom chips dedicated to one narrow function within one circuit design are prohibitively expensive to develop for all but highest volume production runs (in excess of 100,000). The one-chip, one-product notion is attractive, but for moderate volumes or circuit development a compromise is necessary.

The Semi-Customer Is Always Right

The first alternative is the semi-custom chip. These chips fall into two categories: standard cell and gate arrays. The closest in concept to full custom is the standard cell integrated circuit. Various semiconductor manufacturers provide a service for customers to specify such a semi-customised device.

Rather than have to build up a custom circuit from scratch, in the standard cell approach the chip is built up from a library of standard elements. The building blocks include quite complex functions such as RAM, EPROM and CPUs as well as simpler ones such as gates, flip-flops, decoders and multiplexers. Using the semiconductor manufacturer's data on the available circuit elements and computer aided design (CAD) workstations, the customer generates data describing the requirements from which the supplier manufactures the chip.

As in the case of the full custom design, a complete set of masks must be produced for the manufacture of a standard cell device and although design time is shorter, the initial cost is still very high. Accordingly, volume production would once again be required to justify the approach — although the point at which it becomes viable is not quite as high as for the full custom design.

The gate array, or uncommitted logic array (ULA), offers a quite different approach to semi-custom chip design. The basic building block here is nothing more complicated than cells of n-channel and p-channel transistors which can be configured as simple logic gates. Unlike the standard cell, the elements are already etched onto the chip and the customer need only provide interconnection data. Only the mask needs to be produced, for the final, metallisation layer.

Figure 1 shows a typical gate array. It will be noticed that there are two distinct areas on the chip. Around the edges are pads for lead connection and a number of special peripheral cells. These cells, being close to the outside world, are especially suited to provididng I/O interfacing to a variety of other devices.

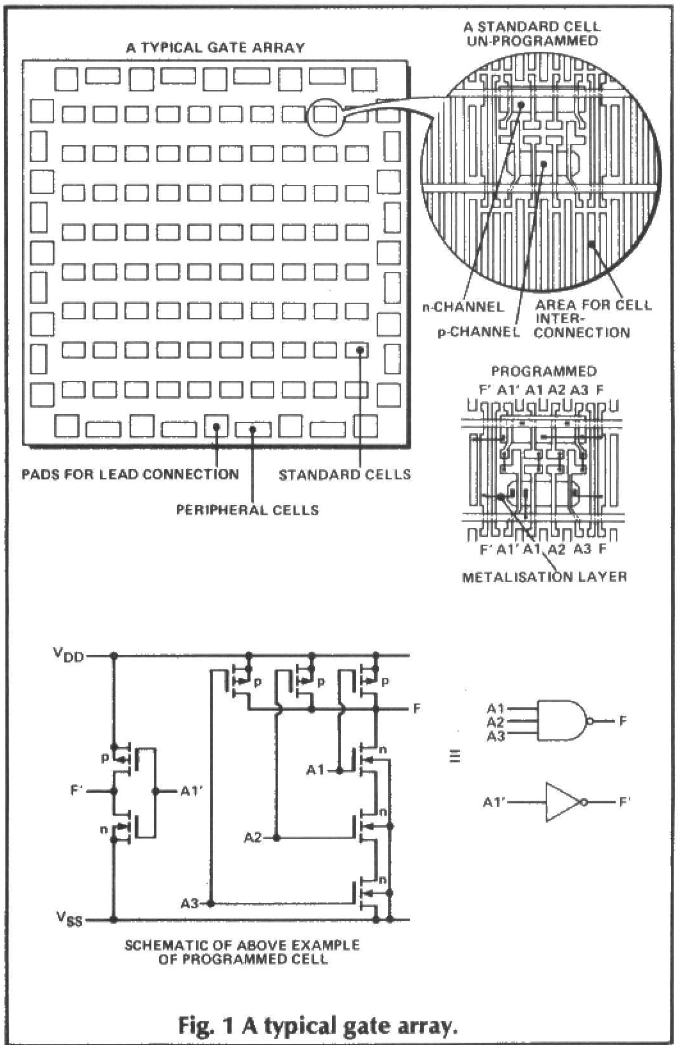


Fig. 1 A typical gate array.

The centre of the chip, on the other hand, is composed of a matrix of standard cells, sometimes thousands in numbers. Figure 1b shows a typical standard cell. The cell has been masked to provide an inverter and a 3-input NAND gate. Conducting strips between the cells are used in conjunction with the mask programming within the cells to provide the required interconnections. Designing interconnections is more involved than in the case of standard cell chips but the initial manufacturing set-up cost of gate arrays is much less and they are, therefore, suited to smaller volumes. Even so, they would not be used for runs of less than a few thousand.

Array Of Hope

Programmable arrays constitute a class of devices which are much less versatile than either custom or semi-custom chips but still provide a high degree of flexibility. Their major advantage is that the semiconductor manufacturer is not involved in the customisation process. Instead, standard devices are obtained and programmed by the customer using equipment similar to a PROM programmer. Initial costs are nowhere near as high as with custom and semi-custom ICs and the devices can be used for relatively small volume production runs. In high volume, the lower initial cost would be more than offset by a higher unit cost. Figure 2 illustrates the varying costs of custom, standard cell, gate array, programmable devices and discrete logic against the volume used.

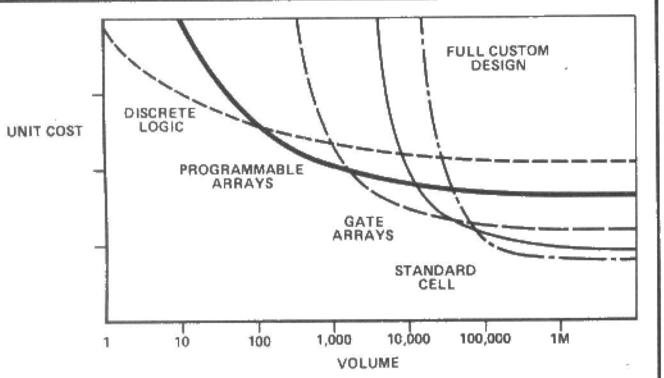


Fig. 2 Price comparison of logic technologies.

Programmable arrays are of three types: PROMs, PALs and FPLAs. The first will be well known to home computer enthusiasts as non-volatile data or program memory chips. The PROM is actually a special case of the programmable AND/OR array. Figure 3 illustrates such an array. The configuration can be used to implement any logic function expressed as a sum of products by selecting appropriate connections into the AND array and out of the OR array. In fact, any Boolean transfer function can be translated to this logic form, given the use of inverters, the only limitations being the number of inputs and outputs.

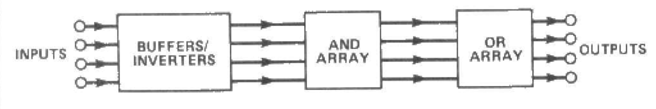


Fig. 3 Generalised AND/OR array.

In order to understand the differences between the various programmable arrays, it is necessary to clarify the notation used in diagrammatic representations of these arrays. Since the gates in any array may well have tens of inputs, for convenience single input lines are used to represent actual multiple inputs (Fig. 4). The figure also shows that two lines crossing in a programmable section of an array represent a fuse programmable link. Fixed sections of an array use the convention of a solid dot to show a connection and crossing lines without a dot to indicate no connection.

PROMs

The characteristic feature of a programmable read-only memory is that the AND array is fixed while the OR array is programmable (Fig. 5). This will be a novel way of looking at a PROM to those who are used to its application as a microrprocessor memory. The Fig. 5 circuit should convince you that this truly is a 4-bit wide, 8-location PROM. In the general case, there will be one AND gate for each combination of inputs (that is, for each location or address) and one OR gate for each output bit.

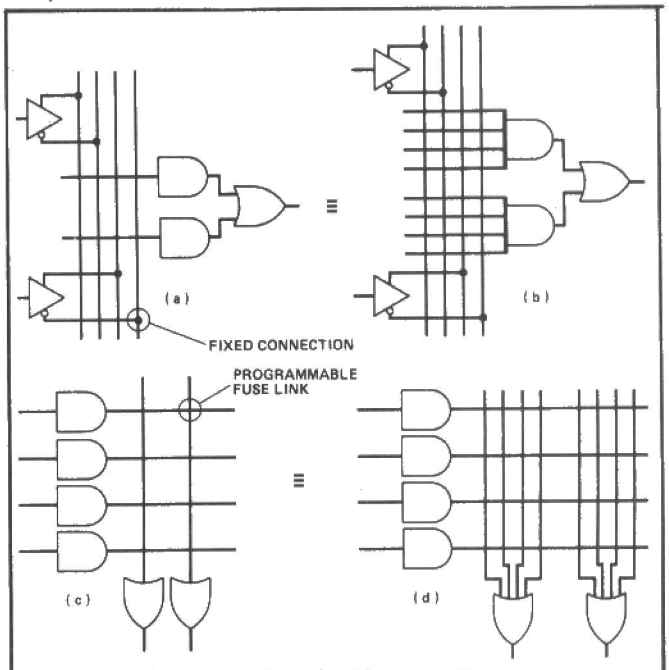


Fig. 4 Notation used in array diagrams.

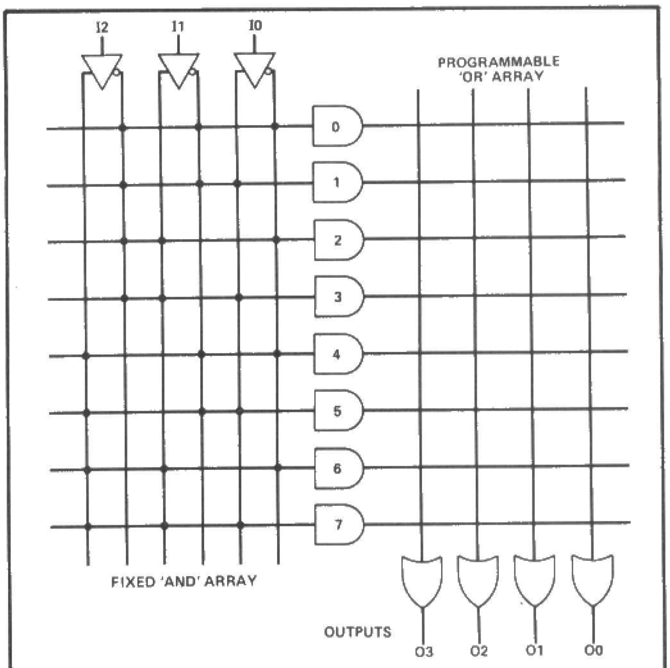


Fig. 5 Typical PROM arrangement (8x4 bits).

PROMs have the advantage of low cost and are relatively easy to program. However, since the AND array is fixed, with one gate for each combination of inputs the chip size increases rapidly with the number of inputs. In fact, the total number of AND gates will be equal to 2 raised to the power of the number of inputs. For example, a 16-input PROM will have 64,000 locations. In the vast majority of applications such a PROM would be heavily under utilised.

A further limitation shows itself in the implementation of state machines. A feedback path is required for each state and, since there is no provision *within* the PROM for feedback, the loop has to be wired externally — using up valuable inputs and outputs. Despite these drawbacks, the PROM does find application as a programmable array, a number of such designs having been presented in ETI in the past (for example, the 64K DRAM Board, ETI, September 1983) primarily in the area of microprocessor address decoding.

FPLAs

The field-programmable logic array (sometimes known by the acronym PLA or IFL, for integrated fuse logic) is illustrated in Fig. 6. It differs from PROMs in that the AND array is programmable as well as the OR array, giving a much greater degree of flexibility. The FPLA does not need a very large array to accommodate a reasonable number of inputs. Further advantages in the form of registered outputs, internal feedback and output polarity are sometimes offered in FPLAs, but since these features are common to PALs, they will be fully covered under that heading.

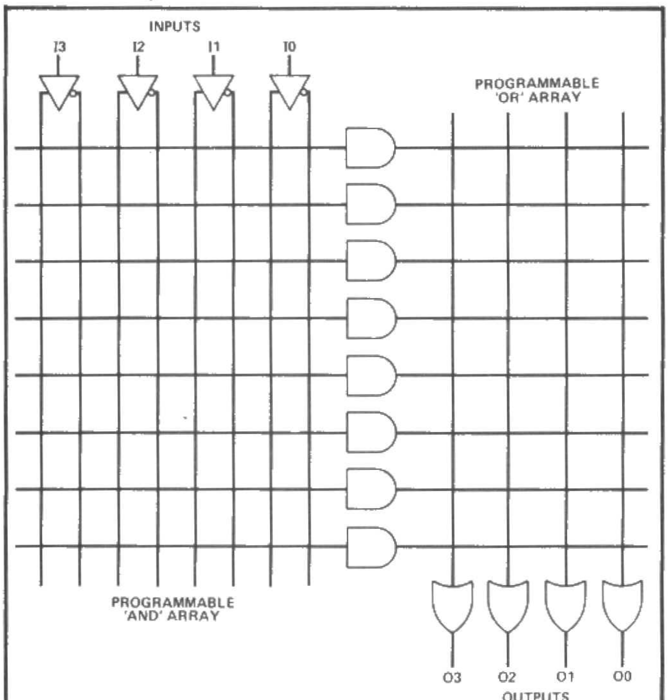


Fig. 6 Typical FPLA arrangement.

Despite these advantages, FPLAs have attracted less interest than PALs, possibly because they are too flexible. The increased flexibility results in longer propagation delays, making FPLAs unsuitable for very high performance designs. All programmable arrays are costly in silicon area, so that if everything is programmable, as with FPLAs, the number of gates is more of a limiting factor. The pros and cons of FPLAs and PALs are hotly debated, the manufacturers of each pushing the advantages of those they supply.

PALs

The PAL configuration (Fig. 7) is the third option for a logic array: a programmable AND array with a fixed OR array. Like FPLAs, PALs provide a number of additional features beyond the basic AND/OR structure. The previously mentioned limitation of PROM architecture due to the fixed number of inputs is overcome in many PALs by use of bi-directional outputs (Fig. 8).

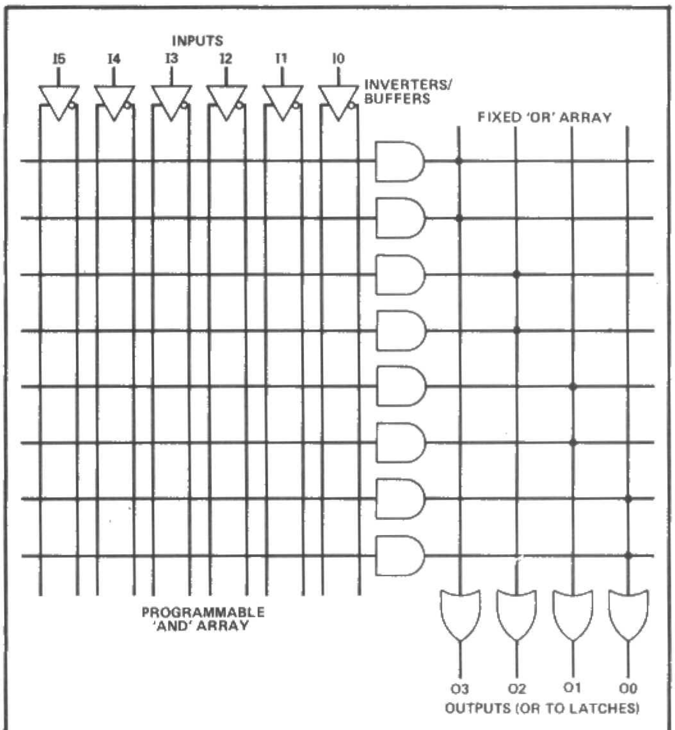


Fig. 7 Typical PAL arrangement.

The output shown in Fig. 8 is fed through a tri-state buffer controlled from the AND array, and so can be disabled. Since a line from this output is fed back to the AND array, the same pin could be used as a further input. It is also possible to provide feedback to the AND array even if the pin in question is being used as an output.

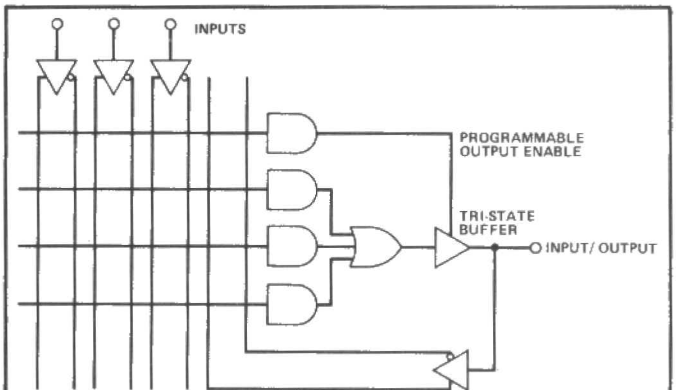


Fig. 8 Bi-directional I/O on a PAL.

A further facility sometimes offered is the use of D-type latches on the outputs to provide a registered output (Fig. 9). Implementations of state machines use internal feedback from this registered output. An output enable may also be provided, controlled from a line common to all outputs on the device.

Programming PALs is not as straightforward as programming PROMs. The procedure is complicated by the fact that it is impossible to address the large number of

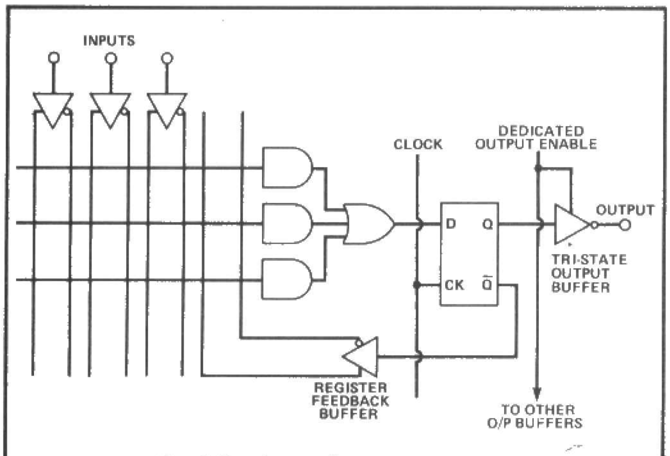


Fig. 9 Registered output on a PAL.

fusible links inside a typical PAL without multiplexing the functions on the limited number of pins. It would not be outside the realms of possibility for an ambitious home constructor to design and build a PAL programmer. Commercial programmers usually have a reasonable degree of intelligence and only require Boolean equations to be entered in order for a fuse map to be worked out automatically. It is outside the scope of an introductory article to go into programming in great depth but the information is of course available from manufacturers' data books.

Applying Some Logic

The application of programmable logic using a PAL can be demonstrated in the simple microcomputer interfacing circuit of a typical low complexity 6809 board (Fig. 10). Discrete TTL logic is used to generate chip select signals for the EPROMs, RAMs, VIA, ACIA and CRTC. Also generated are the $\overline{OE}$ and $\overline{WE}$ signals for the memories and a signal to other boards in the system to indicate that on-board memory is being accessed, which is also used to enable or disable the address and data buffers.

The resultant memory map of this circuit has EPROM 1 at E000 – FFFF, EPROM 2 at C000 – DFFF, RAM 1 at A000 – BFFF, RAM 2 at 8000 – 9FFF and I/O at 6000 – 7FFF. The I/O area is partially decoded to provide addressing for the VIA, ACIA and CRTC. This implementation uses 5 TTL packages, the functions of which may be expressed by the following Boolean equations:

$$\overline{\mathrm{EPROM1}} = \mathrm{A15.A14.A13}$$
$$\overline{\mathrm{EPROM2}} = \mathrm{A15.A14.}\overline{\mathrm{A13}}$$
$$\overline{\mathrm{RAM1}} = \mathrm{A15.}\overline{\mathrm{A14}}\mathrm{.A13}$$
$$\overline{\mathrm{RAM2}} = \mathrm{A15.}\overline{\mathrm{A14}}\mathrm{.}\overline{\mathrm{A13}}$$
$$\overline{\mathrm{VIA}} = \overline{\mathrm{A15}}\mathrm{.A14.A13.A5.A4}$$
$$\overline{\mathrm{ACIA}} = \overline{\mathrm{A15}}\mathrm{.A14.A13.A5.}\overline{\mathrm{A4}}$$
$$\overline{\mathrm{CRTC}} = \mathrm{A15.A14.A13.}\overline{\mathrm{A5}}\mathrm{.A4}$$
$$\overline{\mathrm{OE}} = \mathrm{E.RW}$$
$$\overline{\mathrm{WE}} = \mathrm{E.}\overline{\mathrm{RW}}$$
$$\overline{\mathrm{MEMACC}} = \overline{\mathrm{EPROM1}}.\overline{\mathrm{EPROM2}}.\overline{\mathrm{RAM1}}.\overline{\mathrm{RAM2.VIA}}.\overline{\mathrm{ACIA}}.\overline{\mathrm{CRTC}}$$

These functions may be implemented by a PAL device, reducing the chip count from 5 to 1.

Ten active low non-registered outputs and at least seven inputs are necessary and are available on the 20L10 PAL. Figure 11 is a schematic diagram of this device, programmed for the example application. The program was worked out by hand but it should be quite clear that it will implement the above equations and replace the discrete TTL of the original circuit. This is a simple case, the equations only consisting of ANDed terms so that only one of the inputs of each OR gate is used, the tri-state buffers are always enabled and five of the chip inputs are not used at all.

Programming would not usually be done manually. Instead, a software package would translate the Boolean equations into a fuse map, generating a master tape from which further PALs may be programmed. (Please note that this design is only presented as an example and has not been prototyped and checked in practice.)

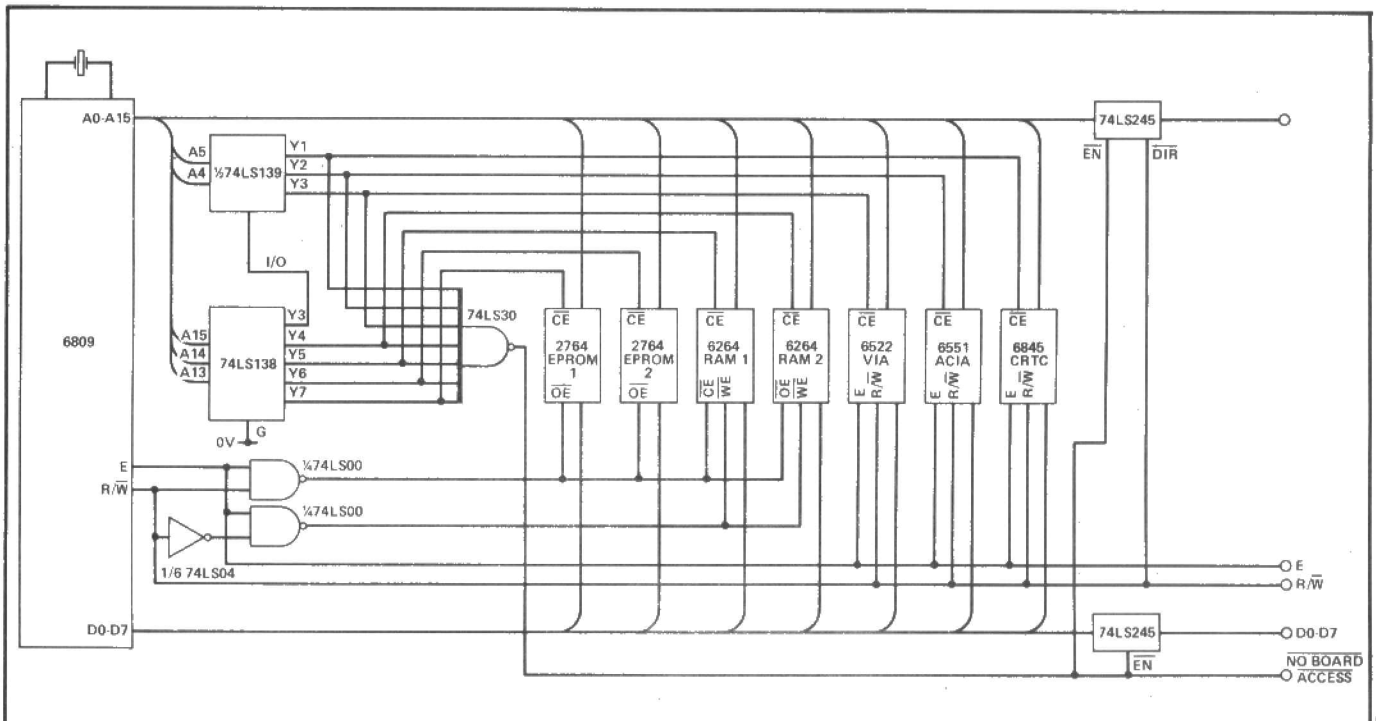


Fig. 10 Simple 6809 board with discrete TTL.

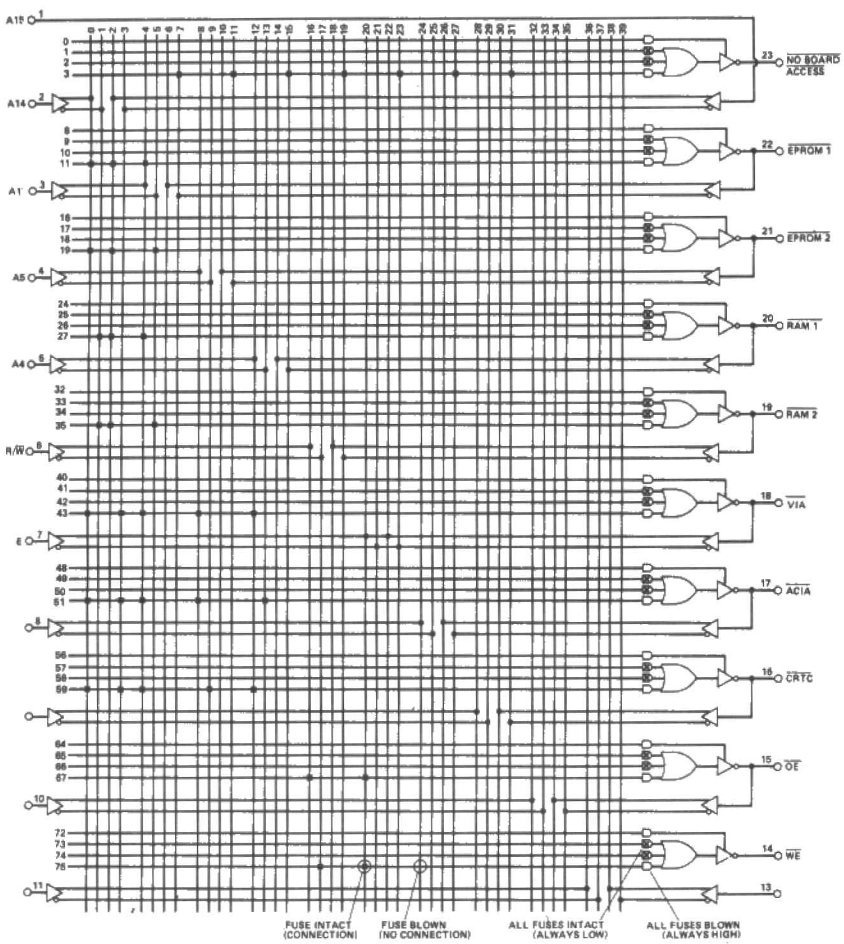


Fig. 11 PAL implementation of 6809 board logic (20L10 PAL).

Recent Developments

Figure 12 sums up the relationships between the various existing logic technologies. Recently, the clear divisions between the various families shown have become much less definite. In particular, the two approaches to semi-customising, standard cell and gate arrays, are beginning to merge. This breakdown of the distinction becomes particularly noticeable to the customer as use is made of increasingly more sophisticated CAD software.

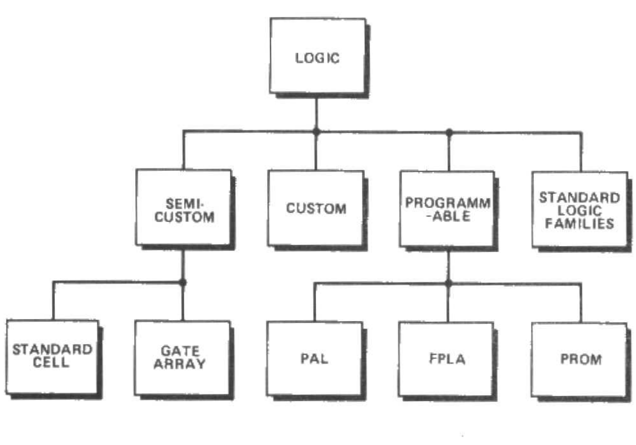


Fig. 12 The families of logic technologies.

The designer of both standard cell or gate array devices is faced with almost indistinguishable development tools, the differences which are transparent being of relevance only at the manufacturing stage. From a customer point of view the only difference is in the price-volume relationship. Performance and interfacing requirements are very similar.

The facilities offered on many recent standard cell libraries and gate arrays are also becoming less distinctive. Gate arrays are now available with much more complex elements than the usual cells of p-channel and n-channel transistors. It is possible to find gate arrays with CPU and memory cells performing functions previously available only in standard cells. From the other side, standard cell libraries may now include blocks of gate arrays to allow last minute customisation and even blocks of PAL to allow modifications after manfuacture. Clearly, these enhancements to gate arrays and standard cells will eventually result in very similar types of semi-custom device.

A further area of recent advance is the development of eraseable programmable logic devices. These have the same relationship to standard PALs and FPLAs as EPROMs have to bipolar PROMs. In full production runs, these devices do not yet provide an economically viable solution to logic design but, in the initial stages of design, they greatly reduce the speed and cost of turning round a series of development versions of a circuit.

Next month, we will feature an experimental project using programmable logic for those wishing to get hands-on experience. **ETI**

PWAyMan MOTOR CONTROLLER

Following a brief mention in his column, Roger Amos expands on the design of a railway modellers' motor controller which makes compromises without sacrifices.

Two techniques have dominated the design of electronic controllers for the DC motors used in model trains and slot racing cars. *Closed-Loop Control* is an analogue technique in which the voltage at the controller's output is compared with a control voltage — in its simplest form this may consist of a power Darlington with its base bias taken from a pot and the load in its emitter circuit. *Pulse width modulation* (PWM) is a digital technique in which the motor is fed pulses whose width is varied to control speed. Normally some form of variable-duty-cycle multivibrator is used to provide an input to a power transistor or thyristor.

Both techniques have their pros and cons, summed up in the table. An ideal controller would combine all the best features and, so far as the laws of thermodynamics permit, eliminate all the problems.

AREA	CLOSED-LOOP	PWM
starting/crawling	good	excellent
motor noise	silent	raucous
motor heating	negligible	a serious problem
output transistor	runs hot	runs cool

The ideal controller would also have another desirable property. Let's face it, most electronic controllers are fairly dumb beasts. They deliver an output that is capable of giving quite fine control of motor speed, but apart from some form of overload protection, rarely do they monitor the motor to see if it is doing what the operator intends. Yet it's not difficult to measure the motor's speed and use this as an input to a feedback loop to lock the motor speed to the control voltage. This would provide compensation for varying loads, when the model negotiates a gradient or tight curve. We would be giving the controller a limited measure of *intelligence*.

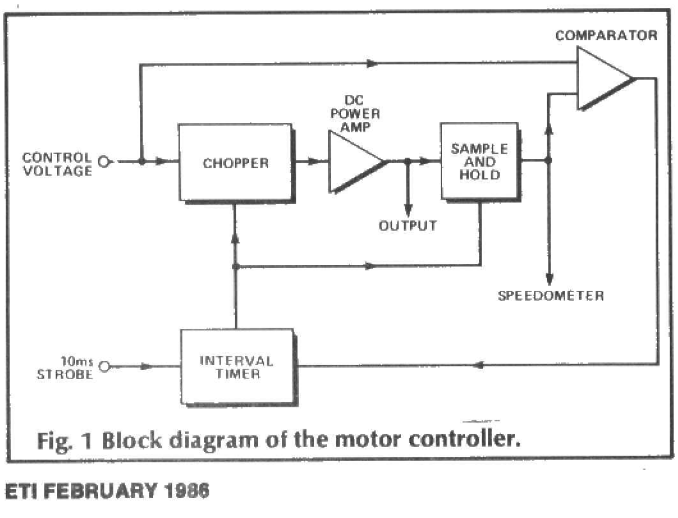


Fig. 1 Block diagram of the motor controller.

The Right Track

My approach was to employ both pulse *width* and pulse *amplitude* modulation. I christened the resultant technique 'Pulse Width and Amplitude Modulation' (PWAM). This acronym reminded me of the railway jargon *'permanent way'* meaning track, so I called the controller the 'PWAyMan'.

The PWAyMan delivers a square-wave PWM output but the pulse amplitude is under direct closed-loop control from the speed control. Pulse width is controlled by a servo which compares the control voltage with the motor EMF. This is measured by a sample-and-hold technique operating during the spaces between pulses. Speed is indicated on a speedometer (Fig.1).

The controller has been extensively tested with a variety of OO-gauge locomotives and found to do all that was required. It gives fine control of speed with very tight speed compensation. A time contant of 2.5s in the servo system makes the controller's response clearly visible — as a train approaches a down gradient it accelerates briefly and then on go the brakes! Give a train a helping pull on its way and the speedometer correctly kicks before the train slows then resumes its original speed. Traction is improved since wheelslips automatically result in counter-action. And impeding a train's progress with a finger automatically raises the duty cycle so the train struggles hard to get away.

Motor noise is quite unobtrusive at low speeds since pulse amplitude is then low. Similarly, no motor heating has been observed, this being proportional to the square of the controller output voltage at low speeds when motor EMF is negligible.

It has two disadvantages. Heat sinkage is still needed for the output device and the circuit is rather complex for a controller. But there's always a price to pay for performance.

Setting up

It is essential for correct operation that the motor EMF monitoring circuit works properly. The best way to check this is by the speedometer. RV3 is used to calibrate this. Different locomotives may need different settings of RV3 until the meter reads 30 (a 100uA movement is assumed). Vary the train speed and you should find that the meter reading varies in proportion. Stalling the loco should bring the reading to zero, as should lifting it off the track. If you have other voltages on the track (such as track circuit voltages), they may cause spurious speedometer readings when there is no loco on the track.

The two LEDs are useful in adjusting the speed servo system. They flash alternately at 100Hz, so fast they they appear to be on together. If they are a well-matched pair, equal brightness will signify a 50 per cent duty cycle. If LED 2 appears brighter, the duty/cycle is greater than 50% and the power pulses are longer. If LED 3 is brighter the pulses are shorter. When incorporated into the controller panel, these LEDs provide a useful indication of the servo action and of the motor loading.

With a train cruising at a moderate speed, adjust feedback control RV2 until the LEDs appear equal in brightness or until the indicated voltage on pin 3 of IC2 is 9V. You should now find that the duty cycle will rise and fall with the load.

Under normal cruising conditions maximum output is about 23V at 50% duty cycle. If you want a higher cruising duty cycle, for running-in a sticky loco, say, all you need do is turn up RV2, but some of the speed compensation will be lost. The controller will still be able to reduce duty cycle when the motor races, but will have less headroom in which to increase it when the load rises. The maximum duty cycle obtainable from the controller is about 85%.

Optional switch SW1 when closed disables the PWM system so the controller functions as a pure DC closed-loop type. This gives higher top speeds and makes the controller compatible with through-the-rails sound systems. But in this mode the speedometer and speed compensation systems do not operate and the LEDs indicate continuous maximum duty cycle.

Input Capabilities

Speed is controlled by the voltage on the slider of speed control RV1. As the controller's input resistance is moderately high (about 25k) it is eminently suitable for use with inertia simulation and automatic control systems. These ramp the control voltage to provide automatic gentle stops and starts.

Power Supply

The prototype was operated from a proprietary transformer delivering 16V AC into a full-wave rectifier consisting of a bridge of four 1N4001s. For correct operation of the PWM system full-wave rectification is essential. An overload cut-out with a threshold of 1A to 2A *must* be fitted to protect transformer, controller and motor against the effects of short circuits or jammed loco mechanisms.

The Circuit

At the heart of the controller is a simple closed-loop voltage follower circuit, Q3 and IC3. The PWM generator uses a 555 timer (IC2) as an interval timer adjustable between nil and 10ms and triggered at 10ms intervals (assuming a 50Hz mains supply) by the nulls in the mains supply waveform. The 555 does not seem to mind having its trigger input taken to 23V or so at the peaks.

The on period of the timer is the length of the *space*, not the power pulse. When the timer is on and its output high it drives transistor Q2 which clamps to ground the input of the closed-loop controller. Since the output of the 555 is high during the trigger pulses themselves, even with the timed interval set to minimum the controller output will be interrupted briefly (in practice for 1.5ms) at 10ms intervals. This is useful since it provides a space during which motor EMF can be sampled even during the highest duty cycles.

The length of the timed period is determined by the network, R2, Q1 and C2. In normal use, this is controlled automatically by the output of the op-amp, IC4. R2 also protects the internal circuitry of the 555 against burnout.

Motor EMF is monitored by the circuitry around Q4, Q5, Q6 and Q7. Q4 and Q5 short-circuit to ground the voltage across the motor (via R8!) during power pulses. Consequently, Q6 and Q7 are permitted to charge C4 up to the motor voltage only during the spaces, when the voltage present can only be motor EMF (which is proportional to motor speed). The *quasi* - Darlington configuration of Q6 and Q7 minimises offset voltage loss and presents a very high input resistance.

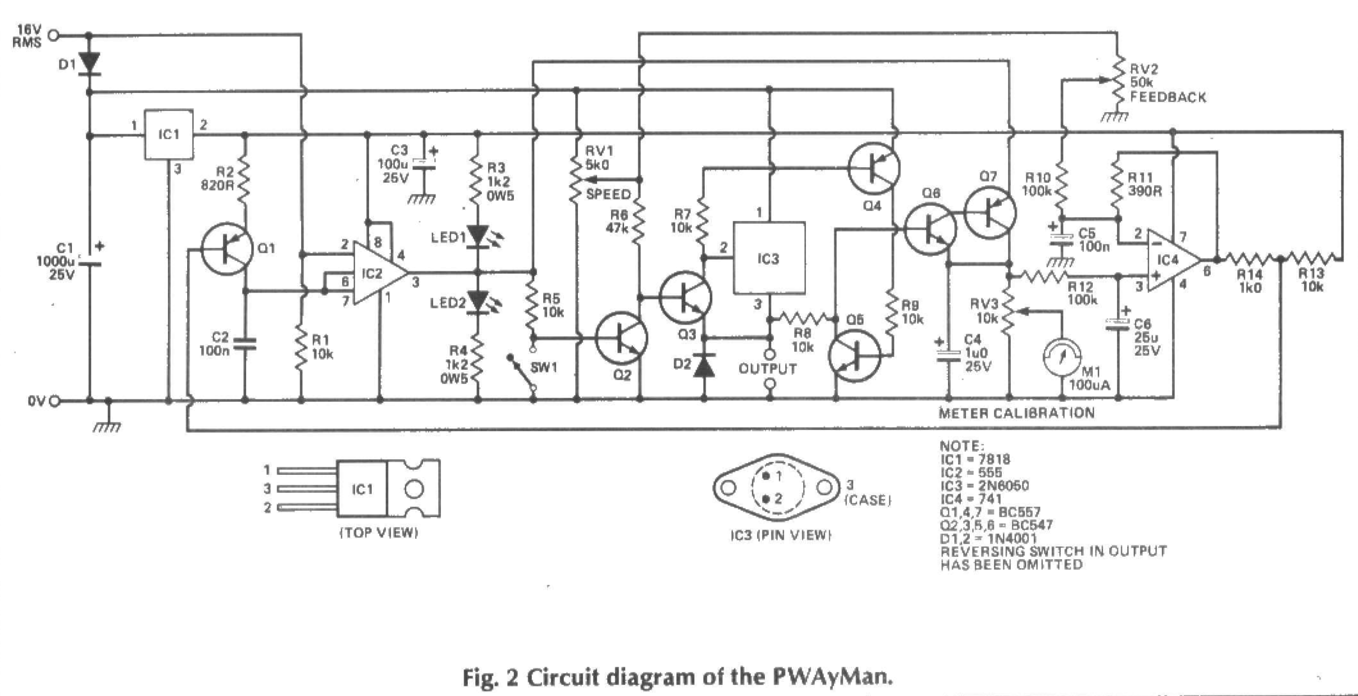


Fig. 2 Circuit diagram of the PWAyMan.

C4 and RV3 are critical and must give a time constant of 10ms. Longer periods cause spurious speedometer readings - shorter ones give inadequate sampling and low readings.

Op-amp IC4 compares the control voltage with the motor EMF and is a 741 set up as an inverting amplifier (from the control voltage viewpoint) with a gain of 4.9. RV2, the feedback control, provides infinitely variable adjustment of the proportion of control voltage that the 741 sees.

As the motor EMF rises relative to the control voltage, so does the 741's output voltage. This biases Q1 back, lengthening IC2's timed period and thereby stabilising its speed.

The ratio of R12 to C6 is important. In the prototype C6 was finalised at 25uF (giving a servo time constant of 2.5s) but this is a matter of taste. It might even be an idea to have a choice of several capacitors selected by a multi-way switch. Too brief a time constant gives the comparator such a rapid response that it counteracts the very pulse width modulation that it is intended to control.

None of the components are critical, with the possible exception of IC3, a PNP power Darlington. The 2N6050 may be hard to get, in which case it could be replaced with an MJ2501, available from Maplin and elsewhere. In fact, any PNP power Darlington with an I_C rating of 4A or more will do.

The CIRCUIT SOLUTION section is designed to provide original design ideas and solutions more comprehensively than TECH TIPS but without the complexitites of a full-scale project. Readers are invited to experiment and design their own stripboard or PCB layouts.

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ELECTRONICS TODAY INTERNATIONAL
FEBRUARY 1986
ADVERTISERS INDEX

CORTEX VIDEO FIX

The Cortex has trouble with its vision systems and Andy Armstrong performs some neat surgery.

Foolishly, perhaps, I offered to do a mod to improve the colour balance on a friend's Cortex. The red was weak and, as a result, there were some colours and backgrounds he didn't use. Fiddling around with the circuitry produced a quick improvement in the colours, but a comprehensive test of the available backgrounds showed that the picture would not lock when bright colours were in use. It bounced continually up and down. Very annoying. On reflection, my friend said it had always done this on one particular video game. And, it turned out, he was not the only one to suffer.

The Sync-ing Feeling

At first I suspected that the UHF modulator was clipping off some of the sync pulse due to non-linearity. Adjusting the bias pot, R37 on the circuit shown (Fig. 1 — which incorporates changes from the original circuit made by kit suppliers Powertran), did not improve matters, however. The next thing I suspected was that I had damaged the sync transistor — Q2, a 2N3906 — so I replaced it. The video now refused to give a locked picture at all!

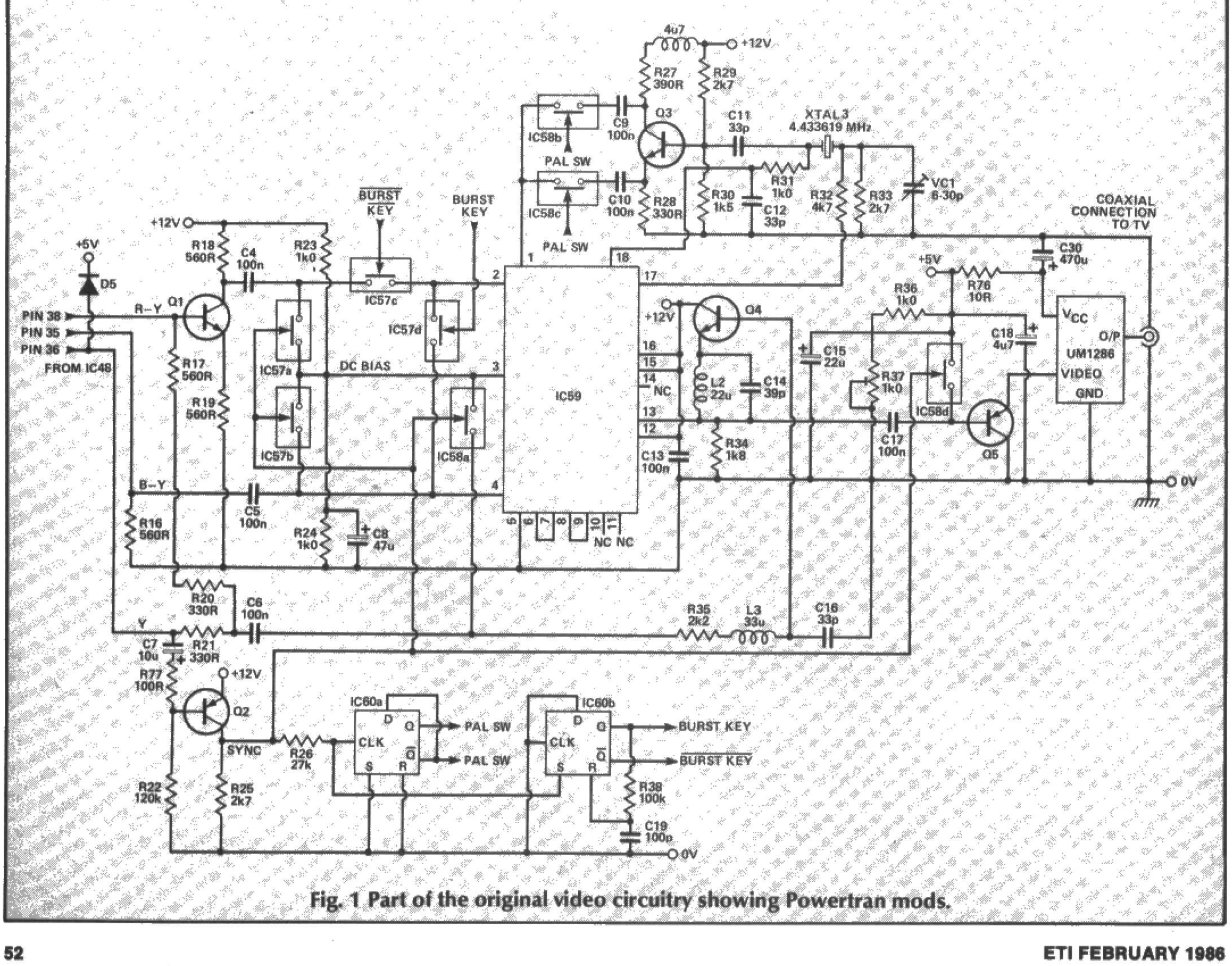


Fig. 1 Part of the original video circuitry showing Powertran mods.

I hadn't got an oscilloscope with me at the time, so the next day — armed with a borrowed 'scope — I set out to discover what was really going on. Tests showed conclusively that the original design was working, partly by luck. The biasing of Q2 was a major part of the problem.

The negative going sync pulse on the Y-signal line from IC48, pin 36, was being heavily loaded by the base-emitter conduction of Q2, which takes place during the sync pulse. This conduction is essential, because the transistor is used to provide a 12V positive going clock pulse when it receives the 0.6V negative going signal on its base. The required base current flow to permit this is only about 400μA, which only needs to occur during the sync pulse. However, because the only DC path to the base of the transistor is via R22, all the charge which enters C7 via R22 during the visible part of the video line must flow into the base of Q2 during the sync pulse.

The current during this period, with the value of R22 given in the original circuit, is much greater than 400μA, and the loading on the Y-signal line during the sync pulse is heavy in consequence.

The first solution I tried is shown in Fig. 2. The pot setting required is affected by the gain of the particular sample of Q2. If an oscilloscope is available, the pot resistance should be increased until the positive going pulse on the collector of Q2 is slightly reduced in amplitude, and then decreased a little bit. If an oscilloscope is not available, then the pot should be adjusted to produce a good picture.

After making this solution work, I wondered about temperature induced drift in the transistor characteristics, and came up with another circuit (Fig. 3). This adjusts the transistor bias according to the amplitude and time of the pulse on the collector of the transistor. The values are chosen to give good performance with an average transistor and to work well with most or all samples. Extreme variations might cause multiple or no clocking of the flip-flop, IC60a, which gives rise to random flashes of colour. The Fig. 3 circuit might be best if an oscilloscope is not available.

Pretty Colours

The remaining problem was to improve the quality of the colours. The circuit of Fig. 4 shows the method used to increase the R-Y gain without upsetting the bias. In order to assess the perfomrance, we used a program which paints colour bars on the screen, and displayed one bar of each colour, with only one pixel between them. It was then easy to adjust the 10k pot, to achieve maximum contrast between the different shades of red and of green.

Postscript

My friend recently showed me copies of a users' magazine, in which several readers had written in with the same problem of vertical jitter on the picture. This decided me to write up the solution. Now, he says that the Cortex performs so well that it should fetch a reasonable second hand price because he wants something bigger and better. (*Is there such a thing? — Ed.*)

The CIRCUIT SOLUTION section is designed to provide original design ideas and solutions more comprehensively than TECH TIPS but without the complexities of a full-scale project. Readers are invited to experiment and design their own stripboard or PCB layouts.

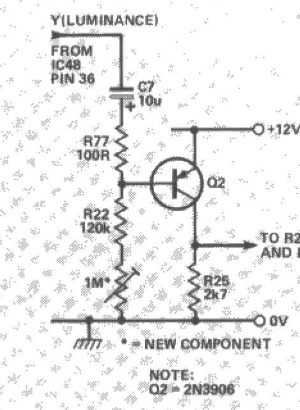


Fig. 2 The fix, part one.

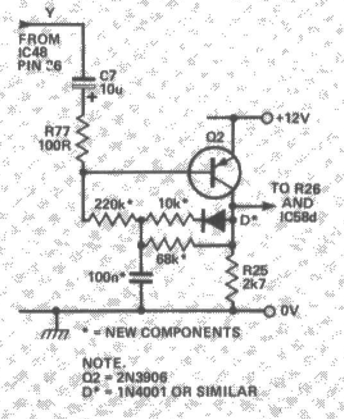


Fig. 3 The fix, part two — overcomes drift and lack of oscilloscope.

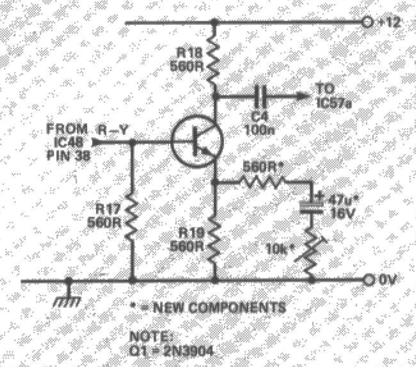


Fig. 4 An added bonus — better colour all round. ETI

SYSTEM A UPDATE

Stan Curtis gives a few hints on how to improve the performance of his original System A design without too much difficulty.

Since the original System A design was first published in ETI, July to September 1981 several thousand pre-amplifiers and over 50 power-amps have been built to my own knowledge based upon sales of PCBs by my company. Inevitably some modifications and improvements came about and the more important of these are listed below. The articles are still available as photocopies and have recently been reprinted in ETI's sister publication, Electronics Digest (Winter 1985, Vol. 6, No. 3).

Pre-Amplifier

1. In a very few cases, high frequency oscillation could occur in the equalisation stage. This is caused by the particular combination of components used by the constructor and should not happen if the recommended parts are used. If it does happen wire a 3p3 min. ceramic capacitor between Q12 base and collector.

2. Due to wiring interactions, there may be high frequency oscillation at some volume settings. This is avoided by wiring a 2k2 resistor between the wiper of RV1 and the junction of R29 and C13. This modification should be made to all pre-amplifiers.

3. The sound quality on the disc inputs can be improved by replacing C12 (10µ tantalum bead) with a 1µ0 100V polyester of the Siemens layer type and by wiring a 1000p 1% polystyrene capacitor in parallel with C3.

4. The pre-amplifier sound is also greatly improved by using good quality metal film resistors throughout (Mullard MR25 and MRS25 are quite suitable).

5. Transistors Q1 and Q2 in the moving-coil stage may be type BD379.

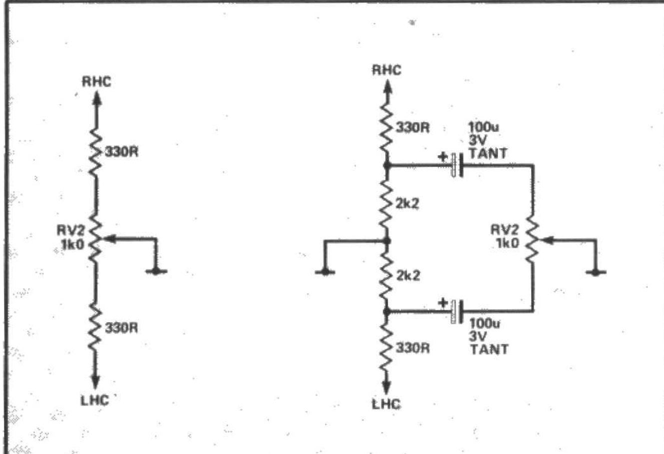


Fig. 1 The balance control, before (left) and after (right).

6. The balance control carries DC current intentionally to ensure that constant resistance is overcome. This does mean that there is an audible brushing noise whenever the control is turned. If this proves an irritation the circuit modification shown in Fig. 1 can be made. The balance control *must* be a wirewound type. Any other type will degrade the stereo separation. In my opinion, this modification worsens the sound quality.

7. The System A pre-amplifier benefits from a generous power supply. The transformer should have a minimum 60VA rating and, if space permits, the reservoir capacitors, C1 and C2 (1000µ), could be increased to 4700µ.

Many constructors prefer to drive each channel of the pre-amplifier from its own regulator (IC1 and IC2) although this involves a modification to the board layout. It is also worth increasing the supply rails to ±18 volts by using 7818 and 7918 regulators and an 18–0–18 volt transformer. Capacitors C2 (1000µ 16V) on the disc modules will then need a 25V rating. No other changes are necessary.

Power Amplifier

1. The sound quality is improved by using 1% 1/4W metal film resistors throughout.

2. With most good loudspeakers it is worth removing the Zobel network (C8, R41) and replacing the output choke (L1, R40) with a 10W wirewound 0R22 resistor.

3. There will be some difficulties in setting up the amplifier unless zener diodes ZD1 and ZD2 are close tolerance types or closely matched to each other.

4. Capacitor C1 can be left out or, if there is a danger of DC offset voltage at the pre-amplifier output, replace it with 1µ0 100 volt polyester.

5. Capacitor C3 should be replaced by a 22p 100V polystyrene type.

6. When setting-up the standard current, the case should be as complete as possible since this affects thermal equilibrium.

7. The heatsinks should be chosen to allow the amplifier to run at a case temperature of between 40 and 50°C. Since each output transistor dissipates 40W, each should be bolted to a heatsink having a rating of less than 1°C/W.

8. The power supply wiring, the output wires and the wires to the output transistors should be as thick as practically possible (at least 2.5mm).

9. Constructors will find it worth resetting the standing current and DC offset voltage after the amplifier has been in use for about ten hours. ETI

TECH TIP

Two Chip Auto-Dialler

Paul Harding
Exeter

When using a modem with a home computer, it is convenient if the computer can dial the destination's number, as is the case with Prestel systems. Although the more expensive modems do this, the cheaper ones do not. The circuit shown here accomplishes the automatic dialling function with a minimum of components.

When READY is high, data on D0 to D3 is loaded into IC1 by briefly taking DIAL High. It should be noted that the circuit does not check that READY is active before accepting the digit data; and if this is not the case, the digit being dialled will be immediately interrupted by the new one, and this will lead to indeterminate numbers being sent. Further, to dial a zero, decimal ten must be loaded.

The flip flop around IC2b and c is set by the DIAL pulse, READY goes low and the oscillator IC2d is enabled. Clock pulses are sent to IC1, causing it to count down, and also to the monostable around IC2e and f, which generates precisely defined output pulses.

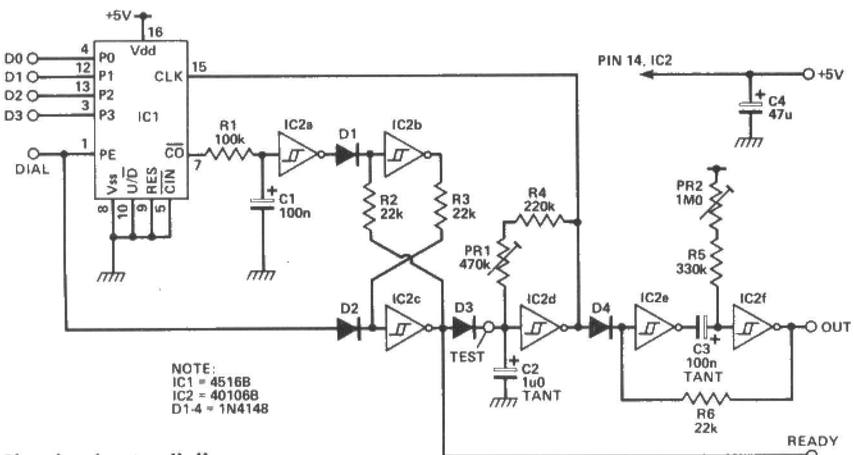
When IC1 finishes its count, $\overline{CO}$ goes low, and, after a short delay produced by R1 and C1 (to ensure that the monostable triggers reliably on the final clock pulse), IC2a resets the flip flop. The oscillator is switched off, and READY returns high, indicating that the next digit can be loaded.

To set the circuit up, the TEST point is cut, allowing the oscillator to free run. Monitoring the output with an oscilloscope, adjust PR1 for a repetition period of 100ms, and PR2 so that the output is high for 60ms every cycle. These figures ensure compatibility with the BT system — but see below. Do not forget to relink the TEST point.

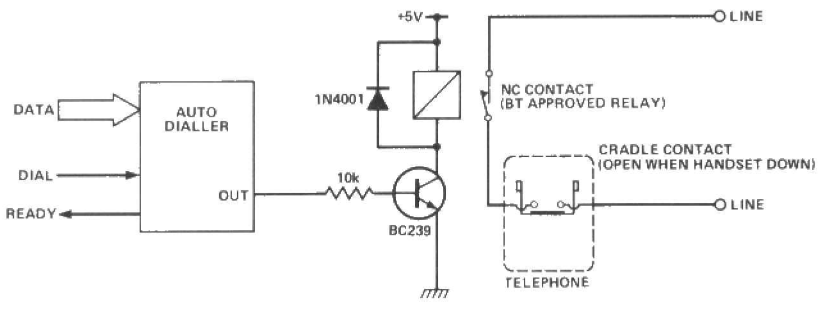
Since the circuit is entirely CMOS, it will run off the computer's power supply without putting the latter under strain. Using a regulated supply will ensure that the oscillator frequency does not drift.

If the circuit is to interface with TTL, low value (about 2k2) pull up resistors will be required on the inputs. They are also desirable if the circuit is not going to be permanently connected to the computer, but in this case can be higher values (100K–1M0). They must be connected to ground in this case.

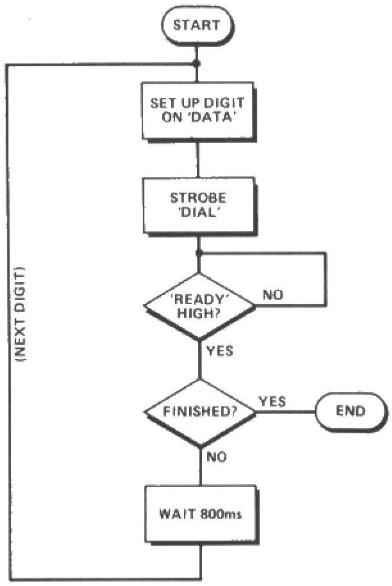
(Note: This circuit must not be connected to British Telecom Lines because it has not gained the required approvals. It can, of course, be connected to private exchanges.)



Circuit of auto-dialler.



Line connection diagram.



Auto-dialler software.

ETI

ETI PCB SERVICE

In order to ensure that you get the correct board, you must quote the reference code when ordering. The code can also be used to identify the year and month in which a particular project appeared: the first two numbers are the year, the third and fourth are the month and the number after the hyphen indicates the particular project.

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E/8411-5	Video Vandal (3 bds)	12.44
E/8411-6	Temperature Controller	3.02
E/8411-7	Mains Failure Alarm	2.63
E/8411-8	Knite Light	3.96
E/8411-9	Stage Lighting Interface	3.74
E/8411-10	Perpetual Pendulum	3.38
E/8412-1	Spectrum Centronics	3.57
E/8412-2	Experimenter's DRAM	14.72
E/8412-3	Active-8: Motherboard	12.22
E/8412-4	Active-8: Protection Unit	3.69
E/8412-5	Active-8: Crossover	3.69
E/8412-6	Active-8: LF EQ	3.69
E/8412-7	Active-8: Equaliser	3.69
E/8412-8	Active-8: Delay Unit	3.69

1985

E/8501-1	Active Bass speaker	2.82
E/8501-2	DRAM Card Update	3.61
E/8501-3	Digital Delay (2 bds)	27.18
E/8502-1	Digital Delay Expander	11.28
E/8502-2	Data Logger	6.21
E/8503-1	Combo preamplifier	4.74
E/8503-2	THD meter mV & osc. bds	7.41
E/8503-3	THD meter mains PSU	3.63
E/8503-4	THD meter battery PSU	1.59
E/8503-5	ParaGraph Equaliser IP/MSP & OP/PSU bds	10.42
E/8503-6	ParaGraph Equaliser filter bd	4.93
E/8504-1	Framestore Memory	12.05
E/8504-2	Framestore ADC/DAC	6.21
E/8504-3	Framestore Control	17.26
E/8504-4	Buzby Meter	3.56
E/8504-5	CCD Delay	3.82
E/8505-1	6802 board	8.22
E/8505-2	EPROM prog. update	5.28
E/8505-3	Scoreboard controller, PSU and opto-isolator bds	POA
E/8505-4	Scoreboard digital driver	4.27
E/8505-5	Stereo Simulator	3.64
E/8506-1	Audio mixer main bd	6.40
E/8506-2	Audio mixer PSU bd	3.98
E/8506-3	Audio mixer RIAA bd	2.62
E/8506-4	Audio mixer tone ctrl	2.85
E/8506-5	EPROM Prog MkII	14.90
E/8507-1	Noise Gate	5.72
E/8508-1	RCL Bridge	12.25
E/8508-2	EX42/BBC Interface	3.25
E/8508-3	EPROM Emulator	POA
E/8509-2	Direct Injection Box	2.90
E/8509-1	SpectROM	POA
E/8510-7	Sorcerer Boards	POA
E/8510-9	Sunrise Light Brightener	6.61
E/8510-8	MTE Power Supply	17.60
E/8511-1	MTE Waveform Generator	4.83
E/8511-2	Millifarodometer	4.69
E/8511-3	Cymbal Synth	6.04
E/8511-4	Memory Scope	10.65
E/8511-5	Chorus Effect	5.16
E/8511-6	Rhythm Chip	*
E/8511-7	Enlarger Exposure Meter	3.86
E/8511-8	Switching Regulator	3.75
E/8511-9	Second Line Of Defence	9.94
E/8512-1	Specdrum Connector	*
E/8512-2	MTE Pulse Generator	6.62
E/8512-3	Specdrum	*
E/8512-4	DI Compression Gate	*

1986

E/8601-1	Autowipe	*
E/8601-2	Walkmate	POA
E/8601-3	MTE Counter/timer	POA
E/8602-1	Digibaro	11.80

* PCB available from another source. See the original article for details.

How to order:

Indicate the boards required by ticking the boxes and send this page, together with your payment, to: ASP Readers' Services, PO Box 35, Wolsey House, Wolsey Road, Hemel Hempstead, Hertfordshire HP2 4SS. For credit card orders, telephone 0442-41221.
Payment in sterling only please. Prices subject to change without notice.

Total for boards £.................... Add 50p p&p   Total enclosed £....................

Signed ....   **Name** ....

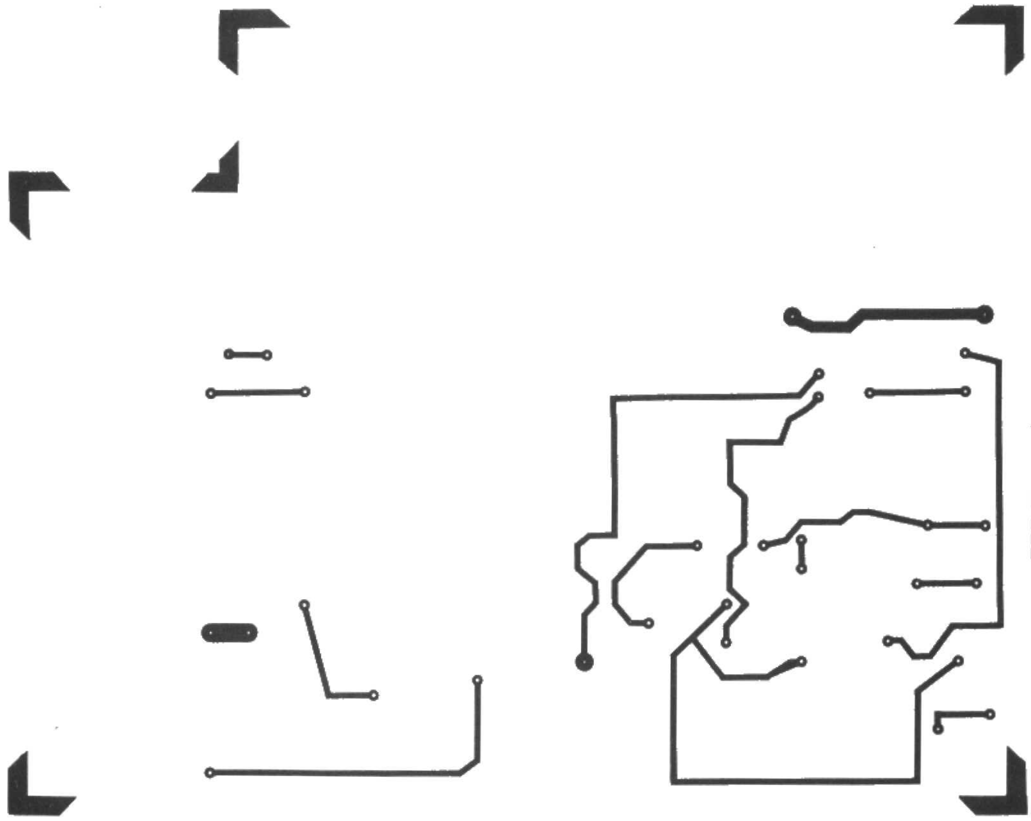
Address ....

....

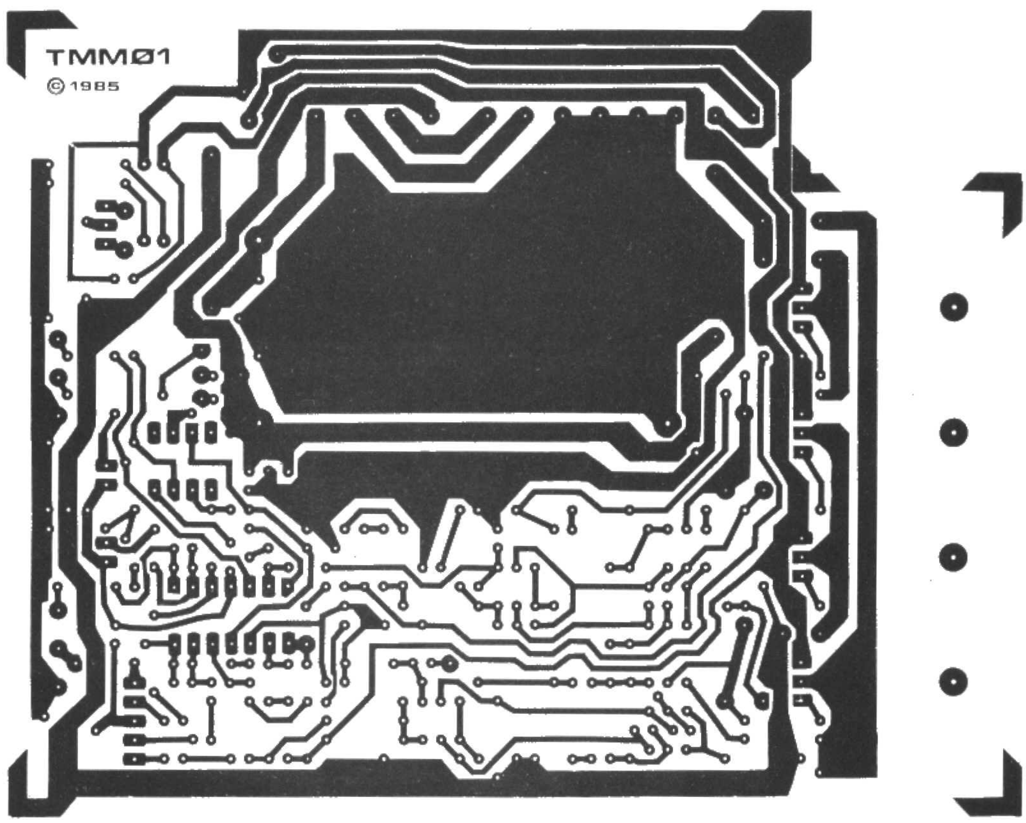
PLEASE ALLOW 28 DAYS FOR DELIVERY

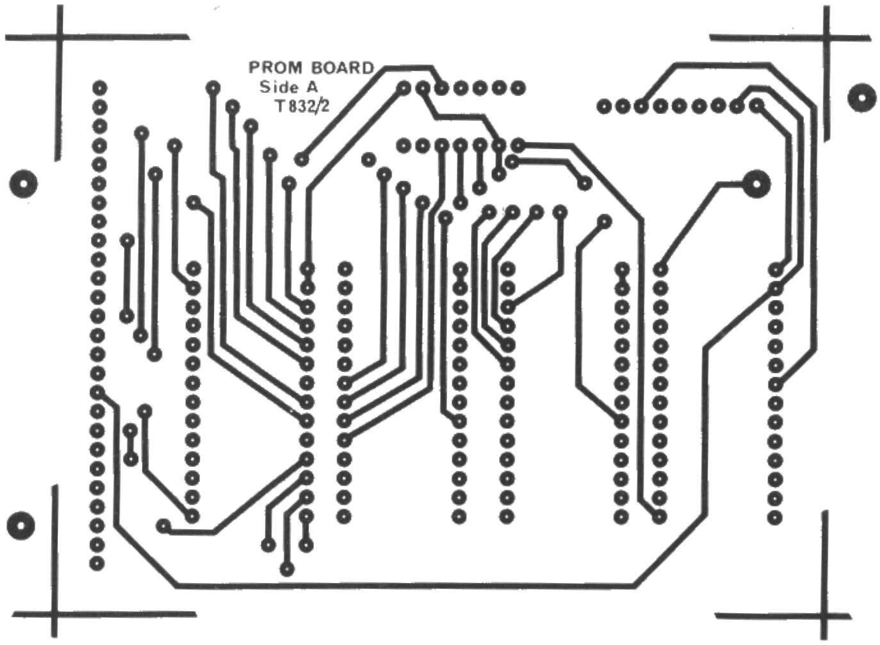
Due to the recent change of manufacturer, a number of boards have not yet been priced. The above list does not include any boards from projects published before the beginning of 1984, although a number of these are still available. All queries as to price and availability should be directed by letter only please to the address shown on this order form.

PCB FOIL PATTERNS

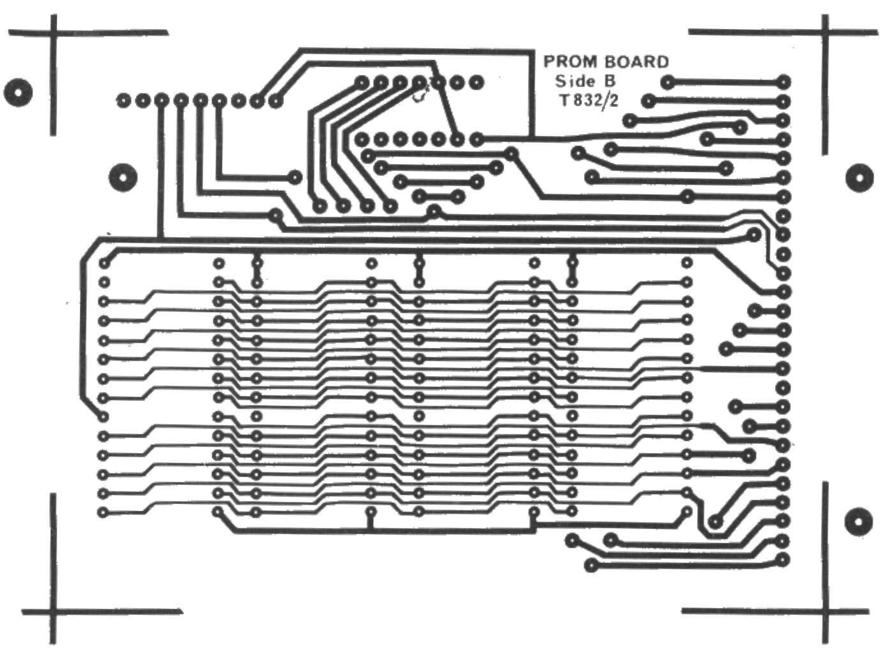


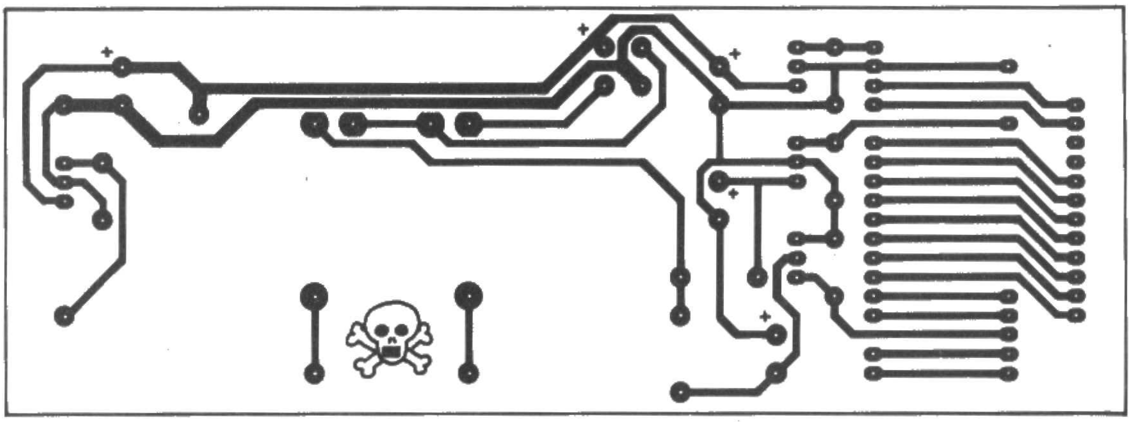
The top and bottom foils for the Microamp board.

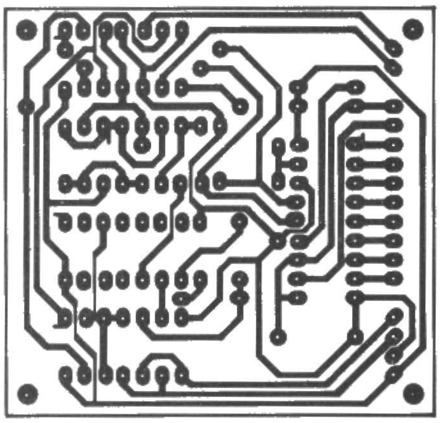


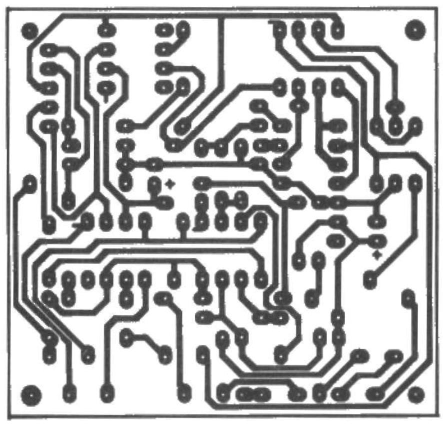


The top and bottom foils for the 6809-based microcomputer EPROM disc board. The foils for the main board are too big to reproduce here but made-up boards are available from Micro Concepts. See the Buylines section in the article.

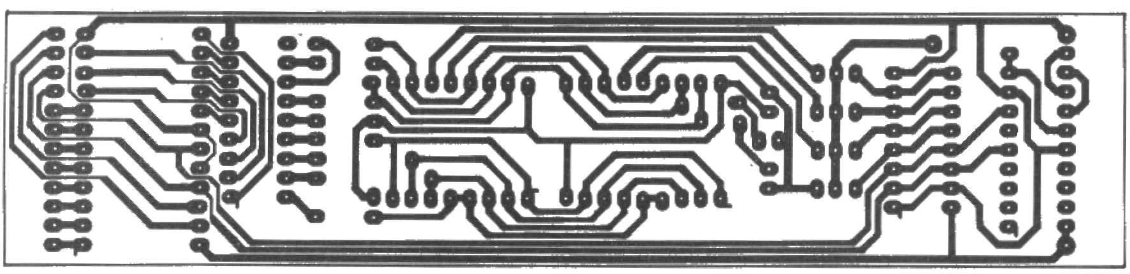








The four foils for the Digibaro.



OPEN CHANNEL

It looks as though we are about to be saddled with 1125-line high-definition television! The October/November meeting of CCIR delegates in Geneva decided to put a proposal before a plenary session of the CCIR in 1986, recommending the adoption of the system as a world-wide standard. This sounds quite innocuous as far as it goes, the only apparent drawback being the paranoid delusions it will engender in the minds of television producers who discover that their programmes will have the potential of a world-wide market. The higher picture and sound quality is also a boon.

But surely all is not that hunky dory. Presently, we have the best television content, that is, the highest programme quality, in the world. You only have to sample the multi-channels of trite tripe available to our North American brethren to know that. I venture to suggest that this is because we have strict regulations regarding the number of channels, amount of advertising, etc. Two developments in television technology could, and most likely would, change all that. The first is that of cable television systems. With cable, many more than our exclusive four channels are piped into our homes, supposedly to let us have a greater choice in what we watch. Great in theory, but lousy in practice. We may have the chance of 20, 30 or more television channels, but what programms do we put on them to watch? Our programme manufacturers couldn't possibly make enough high-quality programmes to fill all those channels. So what would we get? Yes, you've guessed it, many, many imported programmes of trite tripe.

The second development to change our high-quality television content will be the 1125-line world-wide standard. Not only will it be possible for trite tripe programme manufacturers to find slots to place their trite tripe programmes, but it will be technically easier, too, because no conversion is necessary — it's a world-wide standard, remember. So even more trite tripe programmes will find their way into our homes.

Don't misunderstand me, I'm not against the improvement of picture quality that a better television standard will give, it's just the loss of programme quality which worries me. I mean, what's the point of having the potential to view A-rated movies, when all you can actually see are B-rated movies?

The other thing that worries me about a world-wide television standard is who will benefit from manufacturing the television equipment. If you think that British manufacturers will be able to compete successfully with those of other nations then I think you've been watching too many B-rated movies already! It's a Japanese standard and they've already got the equipment on the conveyor belt — we would have to design and develop our own equipment from scratch, or badge-engineer Japanese equipment. Even the large continental manufacturers like Philips will have a hard job competing, so what hope Britain? No, the only way European television manufacturers will be able to survive is to have a European standard, such as the C-MAC system developed and proposed by the IBA. This way the Japanese, and Americans (who have already adopted the 1125-line standard), will not be able to compete effectively because they will be concentrating on their own equipment. We'll also have higher quality television programmes.

Unfortunately, the CCIR is concerned for the most part with the purely technical aspects and the advancement of principles in telecommunications. So the 1125-line high-definition Japanese and American standard will probably become the world standard.

Band II

It's funny, but in a convoluted way, talking about new television standards begs the question about what happens to the old standards. For instance, when the existing 625-line PAL standard came about, what happened to the old 405-line standard. Well, until just a short time ago television transmissions still existed on the radio Band III, so that people with old 405-line receivers (there can't have been that many around) didn't have to rush out (?) and buy one of those new-fangled 625-line tellys. It's ironic that as we are about to make a decision on a new television standard, the last but one is only just closing down. As the decision is made next year on a European or world-wide high-definition television standard, the old Band III is to be re-allocated to other telecommunications services. At least it's a reminder that whatever happens to television communications, there's no rushing the user. And we, as users, can always vote with our feet!

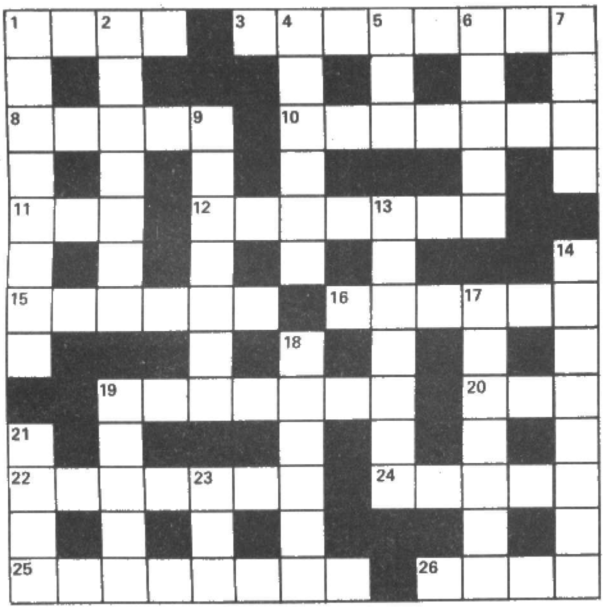
Keith Brindley

ALF'S PUZZLE

The puzzle this month is the whereabouts of the great man himself. We haven't clapped eyes on him since the 'slight disagreement' which resulted when Flea Byte complained about Alf's unscheduled appearance in his Scratchpad column last month. Flea Byte is as well as can be expected and the snipe-nosed pliers have now been surgically removed. The mystery deepens with the arrival this week of an anonymous letter, postmarked Spain. "I never dun it", this mysterious missive informs us, "It was a 4068, and you'll find out why in this month's Digital Superglue article". We will leave readers to draw their own conclusions.

CROSSWORD

No. 1 Solution next month.



ACROSS

1) IF, THEN, , one of BASIC's constructs (4).
2) To send out electromagnetic radiation (8).
8) Cassette access button on a tape recorder (5)
10) Another term for VDU (7).
11) Large manufacturer of magnetic tape (1, 1, 1).
12) A whole number (7).
15) Reuseable memories, usually UV eraseable (6).
16) A power of ten, as in .... counter (6)
19) Whole, independently moveable graphic objects on a computer screen (7).
20) Frequency measuring instrument (1, 1, 1).
22) Large resistive voltage reducer, as found in older television sets (7).
24) FET terminal (5).
25) Sub-atomic particle (8).
26) Print CHR$(7) and this will sound (4).

DOWN

1) A type of small microphone capsule (8).
2) Audio transducer (7).
4) Input on a tape recorder for distant control of on/off switching (6).
5) One of the two bipolar transistor polarities (1, 1, 1).
6) Electrical value indicator (5).
7) One time round on a coil (4).
9) Variable resistor or capacitor (7)
13) Covered with a film of lubrication (7).
14) Connector, often screwdown, for cables (8).
17) One quarter of 4081 CMOS IC? (3, 4).
18) Two-channel audio (6).
19) Abbreviation for a CRT-based test instrument (5).
21) High-to-low or low-to-high voltage transition (4).
23) Abbreviated name for variable resistor (3).

SERVICE SHEET

Enquiries

We receive a very large number of enquiries. Would prospective enquirers please note the following points:

● We undertake to do our best to answer enquiries relating to difficulties with ETI projects, in particular non-working projects, difficulties in obtaining components, and errors that you think we may have made. We do not have the resources to adapt or design projects for readers (other than for publication), nor can we predict the outcome if our projects are used beyond their specifications;

● Where a project has apparently been constructed correctly but does not work, we will need a description of its behaviour and some sensible test readings and drawings of oscillograms if appropriate. With a bit of luck, by taking these measurements you'll discover what's wrong yourself. Please do not send us any hardware (except as a gift!);

● Other than through our letters page, Read/Write, we will not reply to enquiries relating to other types of article in ETI. We *may* make some exceptions where the enquiry is very straightforward or where it is important to electronics as a whole;

● We receive a large number of letters asking if we have published projects for particular items of equipment. Whilst some of these can be answered simply and quickly, others would seem to demand the compiling of a long and detailed list of past projects. To help both you and us, we have made a full index of past ETI projects and features available (see under Backnumbers, below) and we trust that, wherever possible, readers will refer to this before getting in touch with us.

● **We will not reply to queries that are not accompanied by a stamped addressed envelope** (or international reply coupon). **We are not able to answer queries over the telephone.** We try to answer promptly, but we receive so many enquiries that this cannot be guaranteed.

● Be brief and to the point in your enquiries. Much as we enjoy reading your opinions on world affairs, the state of the electronics industry, and so on, it doesn't help our already overloaded enquiries service to have to plough through several pages to find exactly what information you want.

Subscriptions

The prices of ETI subscriptions are as follows;

UK:	£18.10
Overseas:	£22.50 Surface Mail
	$29.50 Surface Mail (USA)
	£49.50 Air Mail

Send your order and money to: ETI Subscriptions Department, Infonet Ltd, Times House, 179 The Marlowes, Hemel Hempstead, Hertfordshire, HP1 1BB (cheques should be made payable to ASP Ltd). Note that we run special offers on subscriptions from time to time (though usually only for UK subscriptions, sorry).

ETI should be available through newsagents, and if readers have difficulty in obtaining issues, we'd like to hear about it.

Backnumbers

Backnumbers of ETI are held for one year only from the date of issue. The cost of each is the current cover price of ETI plus 50p, and orders should be sent to: ETI Backnumbers Department, Infonet Ltd, Times House, 179 The Marlowes, Hemel Hempstead, Hertfordshire HP1 1BB. Cheques, postal orders, etc should be made payable to ASP Ltd. We suggest that you telephone first to make sure there are still stocks of the issue you require: the number is (0442) 48432. Please allow 28 days for delivery.

We would normally expect to have ample stocks of each of the last twelve issues, but obviously, we cannot guarantee this. Where a backnumber proves to be unavailable, or where the issue you require appeared more than a year ago, photocopies of individual articles can be ordered instead. These cost £1.50 (UK or overseas surface mail), irrespective of article length, but note that where an article appeared in several parts each part will be charged as one article. Your request should state clearly the title of the article you require and the month and year in which it appeared. Where an article appeared in several parts you should list these individually. An index listing projects only from 1972 to September 1984 was published in the October 1984 issue and can be ordered in the same way as any other photocopy. If you are interested in features as well as projects you will have to order an index covering the period you require only. A full index for the period from 1972 to March 1977 was published in the April 1977 issue, an index for April 1977 through to the end of 1978 was published in the December 1978 issue, the index for 1979 was published in January 1980, the 1980/81 index in January 1982, the 1982 index in December 1982, the 1983 index in January 1984, the 1984 index in January 1985 and the 1985 index in December 1985. Photocopies should be ordered from: ETI Photocopies, Argus Specialist Publications Ltd, 1 Golden Square, London W1R 3AB. Cheques, postal orders, etc should be made payable to ASP Ltd.

Write For ETI

We are always looking for new contributors to the magazine, and we pay a competitive page rate. If you have built a project or you would like to write a feature on a topic that would interest ETI readers, let us have a description of your proposal, and we'll get back to you to say whether or not we're interested and give you all the boring details. (Don't forget to give us your telephone number).

Trouble With Advertisers

So far as we know, all our advertisers work hard to provide a good service to our readers. However, problems can occur, and in this event you should:

1. Write to the supplier, stating your complaint and asking for a reply. Quote any reference number you may have (in the case of unsatisfactory or incomplete fulfilment of an order) and give full details of the order you sent and when you sent it.
2. Keep a copy of all correspondence.
3. Check your bank statement to see if the cheque you sent has been cashed.
4. If you don't receive a satisfactory reply from the supplier within, say, two weeks, write again, sending your letter recorded delivery, or telephone, and ask what they are doing about your complaint.

If you exhaust the above procedure and still do not obtain a satisfactory response from the supplier, then please drop us a line. We are not able to help directly, because basically the dispute is between you and the supplier, but a letter from us can sometimes help to get the matter sorted out. But please, don't write to us until you have taken all reasonable steps yourself to sort out the problem.

We are a member of the mail order protection scheme, and this means that, subject to certain conditions, if a supplier goes bankrupt or into liquidation between cashing your cheque and supplying the goods for which you have paid, then it may be possible for you to obtain compensation. From time to time, we publish details of the scheme near our classified ads, and you should look there for further details.

OOPS!

Corrections to projects are listed below and normally appear for several months. Large corrections are published just once, after which a note will be inserted to say that a correction exists and that copies can be obtained by sending in an SAE.

Single Board Controller (March 1985)
There were a number of errors in the parts list. RP2 is listed as a 10k SIL pack but is actually four separate resistors, and the same applies to RP3. RP4 is also listed as a SIL pack but should consist of seven commoned resistors. R13 is always required, not just when a cassette interface is used as stated.

The Real Components (May 1985)
In Fig. 1 on page 20, the connections for the Texas L and 2N transistors are incorrectly shown. They should read B, C and E from the top. X

Heat Pen (June 1985)
The instruction in the penultimate paragraph on page 49 should read "... adjust RV2 for 2.73V...", not 2.37V as stated. X

Low Cost Audio Mixer (June 1985)
In Fig. 6 on page 39, the PCB foil pattern has been incorrectly shown as though from the copper side. The board is shown correctly from the copper side in the foil pattern pages. In Fig. 10 on page 40, the positive power rail at lower left should be shown connected to pin 8 of the TL072s, IC1-5). X

Noise About Noise (July 1985)
In Fig. 5 on page 24, no connection should be shown between the cathode of the diode and the negative side of the 470u capacitor. X

Printer Buffer (July 1985)
The case specified is actually larger than the one used for the prototype. It will, of course, work perfectly well, but if you want to a compact unit use a Verocase 202-21038H (180 x 120 x 65mm) rather than a Verocase 202-21035. The regulator IC17 should be bolted to the back of the case to provide heatsinking or, alternatively, fitted with a TO220 heatsink.

Please note that the designer, Nick Sawyer, has been in touch to inform us that the refresh problem we mentioned in September ETI is dealt with in the printer buffer software. In this case there is no need to replace the TMS 4416 dynamic RAMs, although as far as we know the replacement parts mentioned (Hitachi HM48416 DRAMs) will cause no problems. The full text of Nick Sawyer's letter will appear next month. Meanwhile, our apologies for any confusion caused.

Intel 8294 Data Encryption Unit (September 1985)
It should be apparent from the text, page 35, that an actual program has been omitted. This program is for use with the SDK 8085 kit only, and copies may be obtained from us on receipt of a stamped addressed envelope.

Tech Tips — Novel Input Stage (October 1985)
The caption against the lower figure should read "Low noise output at *minimum* gain", not maximum gain. X

Chorus Unit (November 1985)
IC3 is shown on the circuit diagram on page 49 connected to the 9V supply. It should be connected to the 5V supply. The foil pattern connections to this IC are correct. X

Foil Patterns (November 1985)
The foil patterns for the Modular Test Equipment Waveform Generator and the Chorus Unit are shown from the component side rather than the copper side.

X = ALL ADDED TO MAGAZINE WHERE REQUIRED